Freescale Semiconductor Errata (or Chip Errata)

MC33661, Masks M98Z and L06R, Errata

Introduction

This errata sheet applies to part numbers:

- MC33661PEF/R2
- MCZ33661EF/R2

Device Revision Identification

The device revision is indicated by a 1-character code after the device code. For instance the "P" in the MC33661P indicates revision P. All standard devices are marked with device identification and build information code.

Device Build Information / Date Code

Device markings indicate build information containing the week and year of manufacture. The date is coded with the last four characters of the nine character build information code (e.g. "CTZW1025"). The date is coded as four numerical digits, where the first two digits indicate the year and the last two digits indicate the week. For instance, the date code "1025" indicates the 25th week of the year 2010.

Device Part Number Prefixes

Some device samples are marked with a PC prefix. A PC prefix indicates a prototype device which has undergone basic testing only. After full characterization and qualification, devices will be marked with the MC prefix.

General Description

This errata document applies to the MC33661 LIN transceiver IC, powered by SMARTMOS technology.

Errata Type	Meaning
High	Failure mode that severely inhibits the use of the device for all or a majority of intended applications.
Medium	Failure mode that might restrict or limit the use of the device for all or a majority of intended applications.
Low	Unexpected behavior that does not cause significant problems for the intended applications of the device.
Enhancement	Improvement made to the device due to previously found issues on the design.

Table 1. Definitions of Errata Severity

Table 2. Errata for the 33661

Errata No.	Erratum	System Impact	Description				
High Sev	High Severity						
ER01	LIN Dominant Issue	When the anomalous behavior is present, the LIN bus sticks in the 'dominant' state. Communication on the LIN bus is not possible until one of the following conditions occur: 1. 1.V _{SUP} drops below 4.7 V 2. 2.V _{SUP} goes above 5.5V	 The LIN Physical Layer Specification which is part of the LIN Specification Package 2.0 defines the V_{SUP} supply voltage range between 7.0 V and 18 V (V_{BAT} range 8.0 V to 18 V). On this device, the LIN bus output can get stuck in dominant state if both conditions are present: The supply voltage V_{SUP} is below 5.5 V and above 4.7 V (5.5 V > V_{SUP} > 4.7 V). The device is in Normal Mode and the transceiver is forcing the LIN to dominant state (TXD=0V). If V_{SUP} drops further below 4.7 V (Reset threshold typical value), the device will reset and the LIN bus goes in recessive state or if the V_{SUP} is increasing above 5.5 V the LIN bus goes also in recessive state (Normal Operation). Workaround: Avoid stuck condition To avoid the transceiver to transmit data in the critical V _{SUP} area (5.5V to 4.7V), the Low Voltage Interrupt of the Micro Controller can be used to detect the critical V _{SUP} area and to disable (by software) the transmission. To reenable the transmission, the Low Voltage Flag can be used to detect that the supply voltage is back high enough. Remove a stuck condition To avoid having the stuck condition present for a longer period of time, it's possible to detect the dominant state by monitoring the RXD signal. The stuck dominant can be removed by entering the device in Low Power Mode (Sleep Mode) or by preventing the TXD communication transmission (TXD stays in Recessive State) during the V _{SUP} critical voltage range. Fix Plan/Status: None				

Table 2. Errata for the 33661

Errata No.	Erratum	System Impact	Description			
Low Sev	Low Severity					
ER02	LIN BUS driven by TXD when EN is 'low'	When the anomalous behavior is present, the LIN bus will be driven by the state of TXD even if EN is 'low'. When transitioning from Awake into Wait Slow state, the TXD must be 'low', so in this case, the LIN will be driven 'dominant'. In this state, communication on the LIN bus is not possible during the duration of TXD 'low'. Figure 1. and Figure 2.	During the transition into Sleep state (pulling EN pin 'low') and then transitioning into the Awake state by receiving a LIN wake-up pulse or a WAKE pin toggle, the TXD could drive the state of the LIN, even if the EN pin is 'low'. If this occurs and the TXD pin is low, the LIN pin will be driven dominant until the TXD pin goes high. Emperical measurements show that the probability of this anomalous behavior is in the range of 1 out of every 4000 transitions into Sleep state (EN pin pulled 'low'). Root Cause: The anomalous behavior is caused by an asynchronous event when EN is pulled 'low' at about the same time (within a few nanoseconds) as an internal oscillator signal goes 'high'. This creates a race condition of the state machine, and one of the two signals required for the LIN transmitter to be activated does not transition properly, remaining in the enable state. Once the transceiver receives a LIN wake-up pulse or the WAKE pin is toggled, the other necessary signal to activate the LIN transmitter is triggered and the state of TXD drives the LIN bus, even though it should be disabled. It should also be noted that when the issue occurs, the sleep current (I _{SLEEP}) increases from 8.0 typ. to 71 μA at 13.5 V. When the state machine transitions properly, this extra current draw is not present. Workaround: 1. Ensure the TXD pin is in the "high" state during Sleep and Awake modes. In this case, even if the driver is enabled, a dominant pulse is not present on the bus when the anomalous behavior occurs. The consequence to this method is that it is not be possible to transition the device to the Wait Slow mode, and ultimately Slow mode operation, because TXD needs to be low during Awake mode to transition to the Wait Slow state. 2. When the anomalous behavior is present, the node issuing a wake-up signal on the LIN bus must retry by sending a new wake up signal (in accordance with section 2.6.2 WAKE-UP of the LIN 2.2 specification). This method allows the continued use of Slow mode. Fix Plan/Status: None			





Table 2. Errata for the 33661

Errata No.	Erratum	System Impact	Description
ER03	Transceiver remains in Normal, Slow, or Fast mode after the Toggle function	 When the anomalous behavior is present, the state of the transceiver remains the same after the Toggle function is performed: Transceiver does not transition out of Normal into Fast mode Transceiver does not transition out of Slow into Fast mode Transceiver does not transition out of Fast into Normal mode Transceiver does not transition out of Fast into Normal mode Transceiver does not transition out of Fast into Normal mode 	After performing the Fast Baud Rate Selection (Toggle function), the transceiver could stay in its current state. It does not transition out of Normal, Slow, or Fast mode when the anomalous behavior is present. Per simulation, the probability of this behavior happening is in about 1 out of every 500 transitions into and out of Fast state (Toggle function).
			Root Cause: The anomalous behavior is caused by an asynchronous event when TXD is pulled 'high' at about the same time (within a few nanoseconds) as an internal oscillator signal goes 'high'. This creates a race condition of the state machine and the Toggle function signal erroneously goes back to 'low', not allowing the Toggle function transition, so the transceiver remains in its current state.
			Workaround: Repeat the Toggle function if the anomalous behavior is present on the first try, when the transceiver did not transition out of Normal, Slow, or Fast mode.
			Fix Plan/Status: None
ER04	Transceiver transitions into Normal instead of Slow state	When the anomalous behavior is present, the transceiver transitions into Normal from Wait Slow state, instead of into Slow state. Although communication is still possible, the LIN bus transitions are faster	During the transition into Wait Slow state (pulling EN pin 'high'), and then transitioning into Slow state by pulling TXD 'high', the transceiver could go into Normal instead of Slow state. Per simulation, the probability of this happening is about 1 out of every 3000 transitions into Wait Slow state (EN pin pulled 'high').
		(corresponding to the Normal state slew rate timing).	Root Cause: The anomalous behavior is caused by an asynchronous event when EN is pulled 'high' at about the same time (within a few nanoseconds) as an internal oscillator signal goes 'high'. This creates a race condition of the state machine and an internal 'slew rate' signal erroneously stays 'low'. Once the TXD is pulled 'high', the transceiver transitions into Normal instead of Slow state.
			Workaround: There is no workaround.
			The LIN communication is still possible, but at a faster slew rate (Normal state).
			Fix Plan/Status: None

Revision History

Revision	Date	Description
3.0	1/2014	 Added Revision History Updated to new errata format Added ER02, ER03, and ER04



How to Reach Us:

Home Page: freescale.com

Web Support: freescale.com/support Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/SalesTermsandConditions.

Freescale and the Freescale logo are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. SMARTMOS is a trademark of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© 2014 Freescale Semiconductor, Inc.

Document Number: MC33661ER Rev. 3.0 01/2014

