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December 2014

# FSA1208 Low-Power, Eight-Port, High-Speed Isolation Switch

### **Features**

Low On Capacitance: 6 pF Typical
 Low On Resistance: 15 Ω Typical

Low Power Consumption: 1 A Maximum

■ 10 µA Maximum I<sub>CCT</sub> over an Expanded Voltage Range (V<sub>IN</sub>=2.3 V, V<sub>CC</sub>=4.3 V)

■ Wide -3 dB Bandwidth: > 400 MHz

 Packaged in Space-Saving 20-Lead MLP (2.5 x 4.5 mm)

 7.5 kV ESD Rating; >16 kV Power/GND ESD Rating

■ Low C<sub>OFF</sub> Capacitance: 2.5 pF Typical

## **Applications**

DIMM DDR Memory

## **Description**

The FSA1208 is a low-power, eight-port, high-speed switch. This part is configured as a single-pole, single-throw switch and is optimized for isolating a high-speed source, such as a DDR memory bus. The FSA1208 features an extremely low on capacitance  $(C_{ON})$  of 6 pF Superior channel-to-channel crosstalk minimizes interference.

The FSA1208 contains special circuitry on the A & B pins that allows the device to withstand an over-voltage condition. This device is also designed to minimize current consumption even when the control voltage applied to the /OE pin is lower than the supply voltage (V<sub>CC</sub>). Applications include port isolation and switching in DDR memory modules, portable cell phones, PDAs, digital cameras, printers, and notebook computers.

### **Ordering Information**

Part Number	Top Mark	Operating Temperature Range	Package
FSA1208BQX	F1208	-40 to +85°C	20-Lead, Quad, Molded Leadless Package (MLP), 2.5 x 4.5 mm

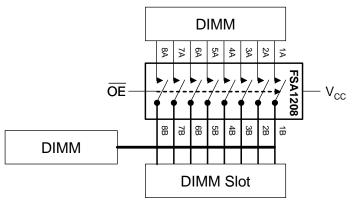
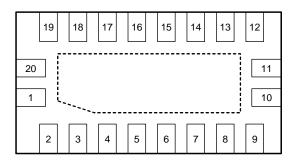


Figure 1. Analog Symbol

# **Pin Configurations**



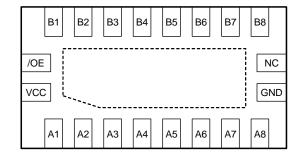


Figure 2. Pin Assignments for MLP (Top Through View)

# **Pin Definitions**

Pin #	Name	Description	
20	/OE	Switch Enable	
2-9	A1-A8	A Side of Bus	
12-19	B8-B1	B Side of Bus	
11	NC	No Connection	
1	VCC	Power	
10	GND	Ground	

# **Truth Table**

/OE	Function
HIGH	Disconnect
LOW	A1-A8=B1-B8

# **Absolute Maximum Ratings**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit	
V <sub>CC</sub>	Supply Voltage		-0.50	+5.25	V
V <sub>CNTRL</sub>	DC Input Voltage (/OE) <sup>(1)</sup>		-0.50	Vcc	V
$V_{SW}$	DC Switch I/O Voltage <sup>(1)</sup>		-0.50	5.25	V
I <sub>IK</sub>	DC Input Diode Current	-50		mA	
I <sub>OUT</sub>	DC Output Current			50	mA
T <sub>STG</sub>	Storage Temperature		-65	+150	°C
		All Pins		7.5	
ESD	Human Body Model, JEDEC: JESD22-A114	I/O to GND		8	kV
LGD		Power to GND		16	ΚV
	Charged Device Model, JEDEC: JESD22-C10		2		

#### Note:

 The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

# **Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
Vcc	Supply Voltage	2.3	4.3	V
V <sub>CNTRL</sub> <sup>(2)</sup>	Control Input Voltage (S, /OE)	0	V <sub>CC</sub>	V
V <sub>SW</sub>	Switch I/O Voltage	-0.5	Vcc	V
T <sub>A</sub>	Operating Temperature	-40	+85	°C

#### Note:

2. The control input must be held HIGH or LOW; it must not float.

### **DC Electrical Characteristics**

All typical values are at 25°C unless otherwise specified.

Complete	Parameter	Conditions	V 00	T <sub>A</sub> =- 40°C to +85°C			Units
Symbol		Conditions	V <sub>cc</sub> (V)	Min.	Тур.	Max.	Jills
V <sub>IK</sub>	Clamp Diode Voltage	I <sub>IN</sub> =-18 mA	2.5			-1.2	V
VIH	Input Voltage High		2.3 to 3.6	1.3			V
VIH	Input Voltage High		4.3	1.7			V
V	Input Voltage Low		2.3 to 3.6			0.5	V
V <sub>IL</sub>	Input Voltage Low		4.3			0.7	V
I <sub>IN</sub>	Control Input Leakage	V <sub>SW</sub> =0 to V <sub>CC</sub>	4.3	-1		1	μA
l <sub>OZ</sub>	Off State Leakage	0 ≤ A, B ≤ 3.6 V	4.3	-2		2	μA
D	Switch On Resistance <sup>(3)</sup>	V <sub>SW</sub> =0 V, I <sub>ON</sub> =-10 mA Figure 3	2.5		7		Ω
R <sub>ON</sub>	Switch Off Resistance	V <sub>SW</sub> =1.8 V, I <sub>ON</sub> =-10 mA Figure 3	2.5		15		Ω
Icc	Quiescent Supply Current	V <sub>IN</sub> =0 or V <sub>CC</sub> , I <sub>OUT</sub> =0	4.3			1	μA
Ісст	Increase in I <sub>CC</sub> Current Per Control Voltage and V <sub>CC</sub>	V <sub>IN</sub> =1.8 V	2.7			10	μΑ

### Note:

### **AC Electrical Characteristics**

All typical values are for V<sub>CC</sub>=2.5 V at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V (\( \)	T <sub>A</sub> =- 40°C to +85°C			Units
	Parameter	Conditions	V <sub>CC</sub> (V)	Min.	Тур.	Max.	Units
t <sub>on</sub>	Turn-On Time, /OE to Output	$R_L$ =50 $\Omega$ , $C_L$ =5 pF $V_{SW}$ =1.8 V Figure 4, Figure 5	2.3 to 3.6		15	34	ns
t <sub>uff</sub>	Turn-Off Time, /OE to Output	$R_L$ =50 $\Omega$ , $C_L$ =5 pF $V_{SW}$ =1.8 V Figure 4, Figure 5	2.3 to 3.6		12	25	ns
t <sub>ad</sub>	Propagation Delay <sup>(4)</sup>	$R_L$ =50 $\Omega$ , $C_L$ =5 pF Figure 4, Figure 6	3.3		0.35		ns
O <sub>IRR</sub>	Off Isolation	$R_L$ =50 Ω, f=400 MHz Figure 11	2.3 to 3.6		-40		dB
Xtalk	Non-Adjacent Channel Crosstalk	$R_L$ =50 Ω, f=100 MHz Figure 12	2.3 to 3.6		-40		dB
BW	0.10.0	$R_L$ =50 $\Omega$ , $C_L$ =0 pF Figure 10	2.3 to 3.6		1000		MHz
DVV	-3dB Bandwidth	$R_L$ =50 $\Omega$ , $C_L$ =5 pF Figure 10	2.3 10 3.0		750		MHz

#### Note:

4. Guaranteed by characterization.

<sup>3.</sup> Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (A or B ports).

# **High-Speed-Related AC Electrical Characteristics**

Symbol	Parameter	Conditions	V (V)	T <sub>A</sub> =- 40°C to +85°C			l Inito
Symbol	Farameter		V <sub>cc</sub> (V)	Min.	Тур.	Max.	Units
t <sub>SK(O)</sub>	Channel-to-Channel Skew <sup>(5)</sup>	C <sub>L</sub> =5 pF	3.3		40	80	ps
t <sub>SK(P)</sub>	Skew of Opposite Transitions of the Same Output <sup>(5)</sup>	C <sub>L</sub> =5 pF	3.3		15	40	ps
t <sub>SK(PKG)</sub>	Package-to-Package Skew <sup>(5)</sup>	C <sub>L</sub> =5 pF	3.3		60	100	ps

### Note:

5. Guaranteed by characterization.

# Capacitance

Symbol	Parameter	Canditions	T <sub>A</sub> =- 40°C to +85°C			Unito
	Parameter	Conditions	Min.	Тур.	Max.	Units
C <sub>IN</sub>	Control Pin Input Capacitance	V <sub>CC</sub> =0.2 V, f=1 MHz		2.0		
Con	D+/D- On Capacitance	V <sub>CC</sub> =2.5 V, /OE=0 V, f=1 MHz Figure 9		6.0		pF
C <sub>OFF</sub>	D1n, D2n Off Capacitance	V <sub>CC</sub> and /OE=2.5 V, f=1 MHz Figure 8		2.5		

### **Test Diagrams**

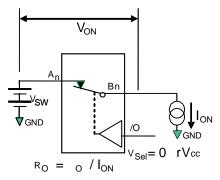
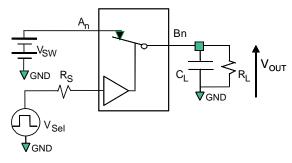


Figure 3. On Resistance



 $R_L$ ,  $R_S$ , and  $C_L$  are functions of the application environment (see AC tables for specific values).  $C_L$  includes test fixture and stray capacitance.

Figure 4. AC Test Circuit Load

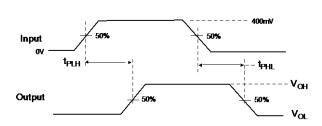


Figure 6. Propagation Delay  $(t_{ry}t_o - 500ps)$ 

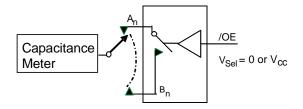


Figure 8. Channel Off Capacitance

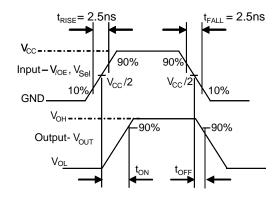


Figure 5. Turn-On / Turn-Off Waveforms

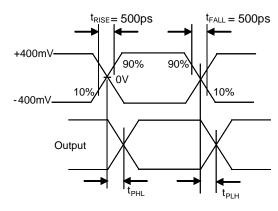


Figure 7. Intra-Pair Skew Test tSK(P)

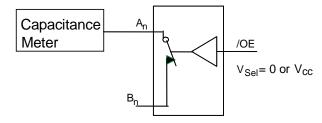


Figure 9. Channel On Capacitance

# Test Diagrams (Continued)

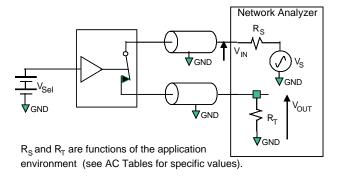


Figure 10. Bandwidth

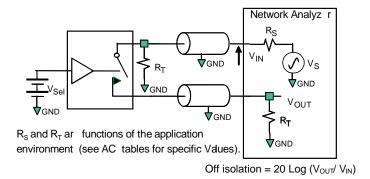


Figure 11. Channel Off Isolation

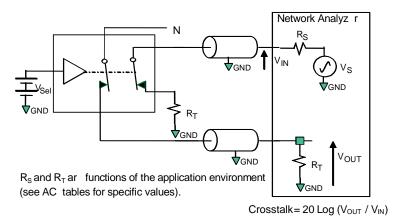
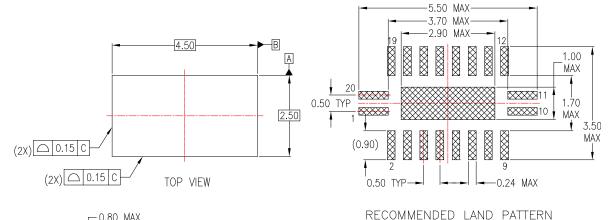
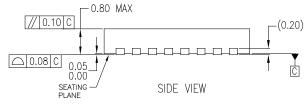
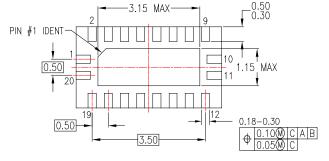


Figure 12. Non-Adjacent Channel-to-Channel Crosstalk

# **Physical Dimensions**







NOTES:

BOTTOM VIEW

- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AC
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP20BrevA

Figure 13. 20-Lead, Molded Leadless Package (MLP)





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