

## **Revision History**

# 2048K x 16bit Low Power CMOS SRAM

# AS6C3216A-55BIN 48ball FBGA PACKAGE

| Revision | Details               | Date         |
|----------|-----------------------|--------------|
| Rev 1.0  | Preliminary datasheet | June 08 2017 |

Alliance Memory Inc. 511 Taylor Way, San Carlos, CA 94070 TEL: (650) 610-6800 FAX: (650) 620-9211 Alliance Memory Inc. reserves the right to change products or specification without notice



## FEATURE

- Fast access time : 55ns
- Low power consumption: Operating current : 12mA (TYP.)
  Standby current : 8µA (TYP.)
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7) UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.2V (MIN.)
- ROHS Compliant
- Package : 48-ball 8mm x 10mm TFBGA

### PRODUCT FAMILY

### **GENERAL DESCRIPTION**

The AS6C3216A-55BIN is a 33,554,432-bit low power CMOS static random access memory organized as 2,097,152 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS6C3216A-55BIN is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The AS6C3216A-55BIN operates from a single power supply of  $2.7V \sim 3.6V$  and all inputs and outputs are fully TTL compatible

| Product         | Operating        |                       | Speed | Power Dissipation               |                                  |  |
|-----------------|------------------|-----------------------|-------|---------------------------------|----------------------------------|--|
| Family          | Temperature      | V <sub>CC</sub> Range | Speed | Standby(I <sub>SB1</sub> ,TYP.) | Operating(I <sub>CC</sub> ,TYP.) |  |
| AS6C3216A-55BIN | <b>-40 ~ 85℃</b> | 2.7 ~ 3.6V            | 55ns  | 8µA                             | 12mA                             |  |

## FUNCTIONAL BLOCK DIAGRAM



## **PIN DESCRIPTION**

| SYMBOL          | DESCRIPTION         |
|-----------------|---------------------|
| A0 - A20        | Address Inputs      |
| DQ0 - DQ15      | Data Inputs/Outputs |
| CE#, CE2        | Chip Enable Input   |
| WE#             | Write Enable Input  |
| OE#             | Output Enable Input |
| LB#             | Lower Byte Control  |
| UB#             | Upper Byte Control  |
| V <sub>cc</sub> | Power Supply        |
| V <sub>SS</sub> | Ground              |
| NC              | No Connection       |



### **PIN CONFIGURATION**



### **ABSOLUTE MAXIMUM RATINGS\***

| PARAMETER                                     | SYMBOL           | RATING                       | UNIT |
|---|------------------|------------------------------|------|
| Voltage on $V_{CC}$ relative to $V_{SS}$      | V <sub>T1</sub>  | -0.5 to 4.6                  | V    |
| Voltage on any other pin relative to $V_{SS}$ | V <sub>T2</sub>  | -0.5 to V <sub>CC</sub> +0.5 | V    |
| Operating Temperature                         | T <sub>A</sub>   | -40 to 85(I grade)           | °C   |
| Storage Temperature                           | T <sub>STG</sub> | -65 to 150                   | °C   |
| Power Dissipation                             | PD               | 1                            | W    |
| DC Output Current                             | Ι <sub>ΟυΤ</sub> | 50                           | mA   |

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

## TRUTH TABLE

| MODE           | CE# | CE2 | OE# | WE#   | WE# LB# UB# I/O OPERATION<br>DQ0 - DQ7 DQ8 - DQ15 SUPPLY |   | SUPPLY CURRENT   |                  |                                   |
|----------------|-----|-----|-----|-------|--|---|------------------|------------------|-----------------------------------|
| WODE           | CE# | CEZ | OE# | VV L# |  |   | DQ0 - DQ7        | DQ8 - DQ15       | JUPPLI CORRENT                    |
|                | Н   | Х   | Х   | Х     | Х  | Х | High-Z           | High-Z           |                                   |
| Standby        | Х   | L   | Х   | Х     | Х  | Х | High-Z           | High-Z           | I <sub>SB1</sub>                  |
|                | Х   | Х   | Х   | Х     | Н  | Н | High-Z           | High-Z           |                                   |
| Output Disable | L   | Н   | Н   | Н     | L  | Х | High-Z           | High-Z           | I <sub>CC</sub> ,I <sub>CC1</sub> |
|                | L   | Н   | Н   | Н     | Х  | L | High-Z           | High-Z           | ICC, ICC1                         |
|                | L   | Н   | L   | Н     | L  | Н | D <sub>OUT</sub> | High-Z           |                                   |
| Read           | L   | Н   | L   | Н     | Н  | L | High-Z           | D <sub>OUT</sub> | I <sub>CC</sub> ,I <sub>CC1</sub> |
|                | L   | Н   | L   | Н     | L  | L | D <sub>OUT</sub> | D <sub>OUT</sub> |                                   |
|                | L   | Н   | Х   | L     | L  | Н | D <sub>IN</sub>  | High-Z           |                                   |
| Write          | L   | Н   | Х   | L     | Н  | L | High-Z           | D <sub>IN</sub>  | I <sub>CC</sub> ,I <sub>CC1</sub> |
|                | L   | Н   | Х   | L     | L  | L | D <sub>IN</sub>  | D <sub>IN</sub>  |                                   |

Note: H= V<sub>IH</sub>, L= V<sub>IL</sub>, X= Don't care.



## DC ELECTRICAL CHARACTERISTICS

| PARAMETER                 | SYMBOL             | TEST CONDITION   |             | MIN.  | <b>TYP.</b> *4 | MAX.                 | UNIT |
|---------------------------|--------------------|--|-------------|-------|----------------|----------------------|------|
| Supply Voltage            | V <sub>cc</sub>    |  | 2.7         | 3.0   | 3.6            | V                    |      |
| Input High Voltage        | V <sub>IH</sub> *1 |  |             | 2.2   | -              | V <sub>CC</sub> +0.3 | V    |
| Input Low Voltage         | V <sub>IL</sub> *2 |  |             | - 0.2 | -              | 0.6                  | V    |
| Input Leakage Current     | ILI                | $V_{CC} \ge V_{IN} \ge V_{SS}$   |             | - 1   | -              | 1                    | μA   |
| Output Leakage<br>Current | I <sub>LO</sub>    | V <sub>CC</sub> ≧V <sub>OUT</sub> ≧V <sub>SS</sub><br>Output Disabled  |             | - 1   | -              | 1                    | μA   |
| Output High Voltage       | V <sub>OH</sub>    | I <sub>OH</sub> = -1mA   |             | 2.2   | 2.7            | -                    | V    |
| Output Low Voltage        | V <sub>OL</sub>    | I <sub>OL</sub> = 2mA  |             | -     | -              | 0.4                  | V    |
| Average Operating         | Icc                | Cycle time = MIN.<br>CE# $\leq$ 0.2V and CE2 $\geq$ V <sub>CC</sub> -0.2V,I <sub>I/O</sub> = 0mA<br>Other pins at 0.2V or V <sub>CC</sub> -0.2V    |             | -     | 12             | 20                   | mA   |
| Power supply Current      | I <sub>CC1</sub>   | Cycle time = $1\mu$ s<br>CE# $\leq$ 0.2V and CE2 $\geq$ V <sub>CC</sub> -0.2V,I <sub>VO</sub> = 0mA<br>Other pins at 0.2V or V <sub>CC</sub> -0.2V |             | -     | 3              | 5                    | mA   |
| Standby Power             |                    | CE# $\geq$ V <sub>CC</sub> -0.2V or CE2 $\leq$ 0.2V<br>Other pins at 0.2V or V <sub>CC</sub> -0.2V   | <b>40</b> ℃ | -     | 8              | 18                   | μA   |
| Supply Current            | I <sub>SB1</sub>   |  | <b>85</b> ℃ | -     | -              | 80                   | μA   |

Notes:

1.  $V_{IH}(max) = V_{CC} + 2.0V$  for pulse width less than 6ns.

2.  $V_{IL}(min) = V_{SS} - 2.0V$  for pulse width less than 6ns.

3. Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.

4. Typical values, measured at  $V_{CC}$  =  $V_{CC}$ (TYP.) and  $T_A$  = 25°C are included for reference only and are not guaranteed or tested.

### **CAPACITANCE** (T<sub>A</sub> = 25℃ f = 1.0MHz)

| PARAMETER                | SYMBOL           | MIN. | MAX. | UNIT |
|--------------------------|------------------|------|------|------|
| Input Capacitance        | C <sub>IN</sub>  | -    | 8    | pF   |
| Input/Output Capacitance | C <sub>I/O</sub> | -    | 8    | pF   |

Note : These parameters are guaranteed by device characterization, but not production tested.



## AC TEST CONDITIONS

| Input Pulse Levels                       | 0.2V to V <sub>CC</sub> - 0.2V  |
|--|---|
| Input Rise and Fall Times                | 3ns   |
| Input and Output Timing Reference Levels | 1.5V  |
| Output Load                              | С <sub>L</sub> = 30pF + 1TTL, I <sub>OH</sub> /I <sub>OL</sub> = -1mA/2mA |

## AC ELECTRICAL CHARACTERISTICS

#### (1) READ CYCLE

| PARAMETER                          | SYM.               | AS6C3216 | A-55BIN |      |
|------------------------------------|--------------------|----------|---------|------|
| PARAMETER                          | 5 T IVI.           | MIN.     | MAX.    | UNIT |
| Read Cycle Time                    | t <sub>RC</sub>    | 55       | -       | ns   |
| Address Access Time                | t <sub>AA</sub>    | -        | 55      | ns   |
| Chip Enable Access Time            | t <sub>ACE</sub>   | -        | 55      | ns   |
| Output Enable Access Time          | t <sub>OE</sub>    | -        | 30      | ns   |
| Chip Enable to Output in Low-Z     | t <sub>CLZ</sub> * | 10       | -       | ns   |
| Output Enable to Output in Low-Z   | t <sub>OLZ</sub> * | 5        | -       | ns   |
| Chip Disable to Output in High-Z   | t <sub>CHZ</sub> * | -        | 20      | ns   |
| Output Disable to Output in High-Z | t <sub>OHZ</sub> * | -        | 20      | ns   |
| Output Hold from Address Change    | t <sub>он</sub>    | 10       | -       | ns   |
| LB#, UB# Access Time               | t <sub>BA</sub>    | -        | 55      | ns   |
| LB#, UB# to High-Z Output          | t <sub>BHZ</sub> * | -        | 20      | ns   |
| LB#, UB# to Low-Z Output           | t <sub>BLZ</sub> * | 10       | -       | ns   |

#### (2) WRITE CYCLE

| PARAMETER                        | SYM.               | AS6C3216A | A-55BIN | UNIT |
|----------------------------------|--------------------|-----------|---------|------|
| PARAMETER                        | 5 T IVI.           | MIN.      | MAX.    | UNIT |
| Write Cycle Time                 | t <sub>wc</sub>    | 55        | -       | ns   |
| Address Valid to End of Write    | t <sub>AW</sub>    | 50        | -       | ns   |
| Chip Enable to End of Write      | t <sub>CW</sub>    | 50        | -       | ns   |
| Address Set-up Time              | t <sub>AS</sub>    | 0         | -       | ns   |
| Write Pulse Width                | t <sub>WP</sub>    | 45        | -       | ns   |
| Write Recovery Time              | t <sub>WR</sub>    | 0         | -       | ns   |
| Data to Write Time Overlap       | t <sub>DW</sub>    | 25        | -       | ns   |
| Data Hold from End of Write Time | t <sub>DH</sub>    | 0         | -       | ns   |
| Output Active from End of Write  | t <sub>ow</sub> *  | 5         | -       | ns   |
| Write to Output in High-Z        | t <sub>WHZ</sub> * | -         | 20      | ns   |
| LB#, UB# Valid to End of Write   | t <sub>BW</sub>    | 50        | -       | ns   |

\*These parameters are guaranteed by device characterization, but not production tested.



### TIMING WAVEFORMS

#### READ CYCLE 1 (Address Controlled) (1,2)



#### **READ CYCLE 2** (CE# and CE2 and OE# Controlled) (1,3,4,5)



Notes :

1.WE# is high for read cycle.

2.Device is continuously selected OE# = low, CE# = low, CE2 = high, LB# or UB# = low.

3.Address must be valid prior to or coincident with CE# = low, CE2 = high, LB# or UB# = low transition; otherwise t<sub>AA</sub> is the limiting parameter.

 $4.t_{cLZ}$ ,  $t_{BLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  are specified with  $C_L$  = 5pF. Transition is measured ±500mV from steady state.

5.At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{BHZ}$  is less than  $t_{BLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .



WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)





#### WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)



Notes :

1.A write occurs during the overlap of a low CE#, high CE2, low WE#, LB# or UB# = low.

- 2.During a WE# controlled write cycle with OE# low, twp must be greater than twHz + to allow the drivers to turn off and data to be placed on the bus.
- 3.During this period, I/O pins are in the output state, and input signals must not be applied.

4.If the CE#, LB#, UB# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.

5.tow and  $t_{WHZ}$  are specified with C<sub>L</sub> = 5pF. Transition is measured ±500mV from steady state.



## **DATA RETENTION CHARACTERISTICS**

| PARAMETER                              | SYMBOL           | TEST CONDITION   |             |                  | TYP. | MAX. | UNIT |
|--|------------------|--|-------------|------------------|------|------|------|
| V <sub>CC</sub> for Data Retention     | V <sub>DR</sub>  | CE#≧V <sub>CC</sub> - 0.2V or CE2≦0.2V   |             | 1.2              | -    | 3.6  | V    |
| Dete Detention Ourset                  |                  | $V_{CC} = 1.2V$  | <b>40</b> ℃ | -                | 6.5  | 18   | μA   |
| Data Retention Current                 |                  | CE# $\ge$ V <sub>CC</sub> -0.2V or CE2 $\le$ 0.2V<br>Other pins at 0.2V or V <sub>CC</sub> -0.2V | <b>85</b> ℃ | -                | -    | 80   | μA   |
| Chip Disable to Data<br>Retention Time | t <sub>CDR</sub> | See Data Retention Waveforms (below)   |             | 0                | -    | -    | ns   |
| Recovery Time                          | t <sub>R</sub>   |  |             | t <sub>RC⁺</sub> | -    | -    | ns   |

 $t_{RC^*}$  = Read Cycle Time

### DATA RETENTION WAVEFORM

Low V<sub>cc</sub> Data Retention Waveform (1) (CE# controlled)



#### Low V<sub>cc</sub> Data Retention Waveform (2) (CE2 controlled)



#### Low V<sub>cc</sub> Data Retention Waveform (3) (LB#, UB# controlled)





### PACKAGE OUTLINE DIMENSION

#### 48-ball 8mm × 10mm TFBGA Package Outline Dimension





SIDE VIEW









|      | D         | IMENSIC<br>(mm) | N     | DIMENSION<br>(inch) |           |       |  |
|------|-----------|-----------------|-------|---------------------|-----------|-------|--|
| SYM. | MIN.      | NOM.            | MAX.  | MIN.                | NOM.      | MAX.  |  |
| А    |           |                 | 1.40  |                     | 3 <b></b> | 0.055 |  |
| A1   | 0.22      | 0.27            | 0.32  | 0.009               | 0.011     | 0.013 |  |
| A2   | <u></u>   |                 | 1.06  | <u></u>             |           | 0.042 |  |
| b    | 0.30      | 0.35            | 0.40  | 0.012               | 0.014     | 0.016 |  |
| D    | 9.95      | 10.00           | 10.05 | 0.392               | 0.394     | 0.396 |  |
| D1   | 5         | .25 BS          | 0     | 0.207 BSC           |           |       |  |
| Е    | 7.95      | 8.00            | 8.05  | 0.313               | 0.315     | 0.317 |  |
| E1   | 3         | .75 BS          | 0     | 0.148 BSC           |           |       |  |
| SE   | 0.375 TYP |                 |       | 0.015 TYP           |           |       |  |
| SD   | C         | .375 T          | Έ     | 0.015 TYP           |           |       |  |
| e    | C         | .75 BS          | C     | 0                   | .030 BS   | SC    |  |

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER.

2. REFERENCE DOCUMENT : JEDEC MO-207.



## **ORDERING INFORMATION**

| AS6C | 3216A                          | 55                     | В        |                                 | N                                | XX                                   |
|------|--------------------------------|------------------------|----------|---------------------------------|----------------------------------|--------------------------------------|
| SRAM | 3216=2M x 16<br>Bit<br>A=A Die | Access Time<br>55=55ns | B = FBGA | l=Industrial<br>(-40° C~+85° C) | Indicates Pb and<br>Halogen Free | Packing Type<br>None:Tray<br>TR:Reel |



Alliance Memory, Inc. 511 Taylor Way, San Carlos, CA 94070 Tel: 650-610-6800 Fax: 650-620-9211 www.alliancememory.com

Copyright © Alliance Memory All Rights Reserved

© Copyright 2007 Alliance Memory, Inc. All rights reserved. Our three-point logo, our name and Intelliwatt are trademarks or registered trademarks of Alliance. All other brand and product names may be the trademarks of their respective companies. Alliance reserves the right to make changes to this document and its products at any time without notice. Alliance assumes no responsibility for any errors that may appear in this document. The data contained herein represents Alliance's best data and/or estimates at the time of issuance. Alliance reserves the right to change or correct this data at any time, without notice. If the product described herein is under development, significant changes to these specifications are possible. The information in this product data sheet is intended to be general descriptive information for potential customers and users, and is not intended to operate as, or provide, any guarantee or warrantee to any user or customer. Alliance does not assume any responsibility or liability arising out of the application or use of any product described herein, and disclaims any express or implied warranties related to the sale and/or use of Alliance products including liability or warranties related to fitness for a particular purpose, merchantability, or infringement of any intellectual property rights, except as express agreed to in Alliance's Terms and Conditions of Sale (which are available from Alliance). All sales of Alliance products are made exclusively according to Alliance's Terms and Conditions of Sale. The purchase of products from Alliance does not convey a license under any patent rights, copyrights; mask works rights, trademarks, or any other intellectual property rights of Alliance or third parties. Alliance does not authorize its products for use as critical components in life-supporting systems where a malfunction or failure may reasonably be expected to result in significant injury to the user, and the inclusion of Alliance products in such life-supporting systems implies that the manufacturer assumes all risk of such use and agrees to indemnify Alliance against all claims arising from such use.