SPECIFICATION

SPEC. No. C-Array-a D A T E: 2013 Sep.

То

Non-Controlled Copy

CUSTOMER'S PRODUCT NAME

MULTILAYER CERAMIC CHIP CAPACITORS

CKC Series / Commercial Grade

2 in 1 Array

4 in 1 Array

Please return this specification to TDK representatives.

If orders are placed without returned specification, please allow us to judge that specification is accepted by your side.

RECEIPT CONFIRMATION

DATE: YEAR MONTH DAY

TDK Corporation Sales Electronic Components Sales & Marketing Group TDK-EPC Corporation

Engineering

Ceramic Capacitors Business Group

APPROVED	Person in charge			

APPROVED	CHECKED	Person in charge

1. SCOPE

This specification is applicable to chip type multilayer ceramic capacitors with a priority over the other relevant specifications.

Production places defined in this specification shall be TDK-EPC Corporation Japan,

TDK (Suzhou) Co., Ltd and TDK Components U.S.A. Inc.

EXPLANATORY NOTE:

This specification warrants the quality of the ceramic chip capacitors. The chips should be evaluated or confirmed a state of mounted on your product.

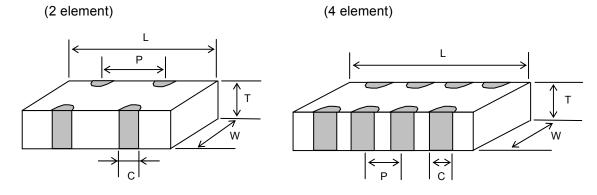
If the use of the chips goes beyond the bounds of the specification, we can not afford to guarantee.

2. CODE CONSTRUCTION

(Example)

Catalog Number :	CKCL22	<u>X5R</u>	<u>0J</u>	<u>105</u>	<u>M</u>	<u>085</u>	<u>A</u>	<u>A</u>
(Web)	CKCA43	<u>X7R</u>	<u>1H</u>	<u>102</u>	M	<u>100</u>	<u>A</u>	<u>A</u>
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
Item Description:	CKCL22	<u>X5R</u>	<u>0J</u>	<u>105</u>	<u>M</u>	<u>T</u>	XXXX	
	CKCA43	<u>X7R</u>	<u>1H</u>	<u>102</u>	<u>M</u>	<u>T</u>	XXXX	
	(1)	(2)	(3)	(4)	(5)	(9)	(10)	

(1) Type



Please refer to product list for the dimension of each product.

(2) Temperature Characteristics (Details are shown in table 1 No.7 at page4 and No.8 at page 5)

(3) Rated Voltage

Symbol	Rated Voltage
1 H	DC 50 V
1 E	DC 25 V
1 C	DC 16 V
1 A	DC 10 V
0 J	DC 6.3 V



(4) Rated Capacitance

Stated in three digits and in units of pico farads (pF).

The first and Second digits identify the first and second significant figures of the capacitance, the third digit identifies the multiplier.

R is designated for a decimal point.

Example 102 \rightarrow 1,000pF

 $105 \rightarrow 1,000,000pF$

(5) Capacitance tolerance

Symbol	Tolerance	Capacitance	
F	± 1 pF	10pF	
K	± 10 %	Over 10pE	
М	± 20 %	Over 10pF	

- (6) Thickness code (Only Catalog Number)
- (7) Package code (Only Catalog Number)
- (8) Special code (Only Catalog Number)

(9) Packaging (Only Item Description)

Symbol	Packaging		
В	Bulk		
Т	Taping		

(10) Internal code (Only Item Description)

3. RATED CAPACITANCE AND CAPACITANCE TOLERANCE

3.1 Standard combination of rated capacitance and tolerances

Class	Temperature Characteristics	Capacitance tolerance	Rated capacitance
4	СН	F (± 1pF)	10pF
1	C0G	K (± 10 %)	E – 6 series
2	J B X5R X7R X8R	M (± 20 %)	E – 3 series

3.2 Capacitance Step in E series

E series	Capacitance Step						
E- 3	1	.0	2	.2	4.7		
E- 6	1.0 1.5		2.2	3.3	4.7	6.8	

4. OPERATING TEMPERATURE RANGE

T.C.	Min. operating Temperature	Max. operating Temperature	Reference Temperature
C H J B	-25°C	85°C	20°C
X5R	-55°C	85°C	25°C
X7R C0G	-55°C	125°C	25°C
X8R	-55°C	150°C	25°C

5. STORING CONDITION AND TERM

5 to 40°C at 20 to 70%RH

6 months Max.

6. INDUSTRIAL WASTE DISPOSAL

Dispose this product as industrial waste in accordance with the Industrial Waste Law.



7. PERFORMANCE

table 1

No.	Item	Perfo	ormance	Test	or inspection	method	
1	External	No defects which	may affect	Inspect with magnifying glass (3×)			
	Appearance	performance.					
2	Insulation	10,000MΩ min.		To measure between each terminal.			
	Resistance	1 '	tors of rated voltage	Apply rated	voltage for 6	0s.	
		16, 10, 6.3V DC, 2 whichever smaller	•				
3	Voltage Proof	Withstand test vol					
3	Voltage Frooi	insulation breakdo	_	Class	Apply	voltage	
		damage.		Class1		d voltage	
				Class2		ed voltage	
				Above DC v	oltage shall b	ne annlied	
					terminal for	• •	
				Charge / dis	charge curre	nt shall not	
			exceed 50m	nA.			
4	Capacitance	Within the specifie					
			Class	Measuring frequency	Measuring voltage		
			Class1	1MHz±10%	0.5-5 Vrms.		
					1kHz±10%	1.0±0.2Vrms	
				To measure between each terminal.			
5	Q			See No.4 in	this table for	measuring	
	(Class1)	Spec	ification	condition.			
		30pF and over	-				
		Under 30pF	Q ≥ 400+20·C				
		C : Rated capacita	ance (pF)				
6	Dissipation Factor			See No.4 in	this table for	measuring	
	(Class2)	T.C.	D.F.	condition.			
		JB	0.025 max.				
		X5R X7R	0.03 max. 0.05 max.				
		X8R	0.03 max.				
7	Temperature			Tomporature	e coefficient s	shall bo	
,	Characteristics of	T.C. Temperature Coefficient C H $0 \pm 60 \text{ (ppm/°C)}$ C0G $0 \pm 30 \text{ (ppm/°C)}$		· •	ased on valu		
	Capacitance			and 85°C temperature. Measuring temperature below 20°C shall be -10°C and -25°C.			
	(Class1)						
		Capacitance dri		3 4.14 20 0	-		



No.	Item	Performance	Test or inspection method
8	Temperature Characteristics of Capacitance (Class2)	Capacitance Change (%) No voltage applied J B: ± 10 X5R: ± 15 X7R: ± 15 X8R: ± 15	Capacitance shall be measured by the steps shown in the following table after thermal equilibrium is obtained for each step. ΔC be calculated ref. STEP3 reading Step Temperature(°C) 1 Reference temp. ± 2 2 Min. operating temp. ± 3 3 Reference temp. ± 2
9	Robustness of Terminations	No sign of termination coming off, breakage of ceramic, or other abnormal signs.	Reflow solder the capacitors on a P.C.Board shown in Appendix1 to 3 and apply a pushing force of 5N with 10±1s.
10	Solderability	New solder to cover over 75% of termination. 25% may have pin holes or rough spots but not concentrated in one spot. Ceramic surface of A sections shall not be exposed due to melting or shifting of termination material. A section	Completely soak both terminations in solder at 235±5°C for 2±0.5s. Solder: H63A (JIS Z 3282) Flux: Isopropyl alcohol (JIS K 8839) Rosin (JIS K 5902) 25% solid solution.

No.	Ite	em		Perfo	ormance		Test or inspection m	nethod																
11	Vibration	External appearance	No mech	anical o	damage.	P.C.B	v solder the capacitor pard shown in Appen																	
		Capacitance	Characte	eristics	Change from the value before test		e testing. e the capacitors with	with amplitude of																
			Class1	C H C0G	±2.5% or ±0.25pF, whichever larger.	1.5mn	n P-P changing the fr 0Hz to 55Hz and bac	equencies																
			Class2	J B X5R X7R X8R	± 7.5 %	about Repea																		
		Q																						
		(Class1)	Rat Capac		Q																			
	D.F. (Class		30pF ar	nd over	1,000 min.																			
			Under 3	30pF	400+20×C min.																			
			C : Rated capacitance (pF)																					
		D.F. (Class2)	Meet the initial spec.																					
12	12 Temperature cycle	External appearance	No mechanical damage.			Reflow solder the capacitors on a P.C.Board shown in Appendix 1 to 3																		
		Capacitance				before testing.																		
			Characte	eristics	Change from the value before test	Expose the capacitors in the condition step1 through step 4 and repeat 5 time consecutively. Leave the capacitors in ambient condition for 6 to 24h (Class 1) or 24 to 2h (Class 2) before measurement.																		
			Class1	C H C0G	±2.5% or ±0.25pF, whichever larger.																			
			Class2	J B X5R X7R X8R	± 7.5 %																			
		0						T																
		Q (Class1)																	Rat Capac		Q	Step	Temperature(°C) Min. operating temp.	Time (min.)
			30pF ar	nd over	1,000 min.	1	per para.4. ± 3	30 ± 3																
			Under 3	80pF	400+20×C min.	2	Reference temp. per para.4.	2 - 5																
			C : Rated capacitance (pF)			3	Max. operating	30 ± 2																
		D.F. (Class2)	Meet the	initial s	spec.	4	Reference temp. per para.4. ± 2	2 - 5																
		Insulation Resistance	Meet the	initial s	spec.		- Para. 1.	<u> </u>																
		Voltage proof	No insula damage.	tion bre	eakdown or other																			

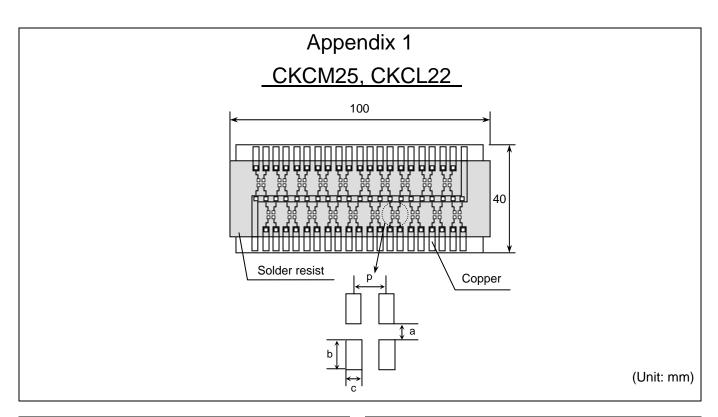
No.	It	em	Performance			Test or inspection method	
13	Moisture Resistance	External appearance	No mecha	nical da	amage.	Reflow solder the capacitors on a P.C.Board shown in Appendix 1 to 3	
	(Steady State)	Capacitance	Charact	eristics	Change from the value before test	before testing.	
			Class1	C H C0G	±5% or ±0.5pF, whichever larger.	Leave at temperature 40 ± 2°C, 90 to 95%RH for 500 +24,0h.	
			Class2	J B X5R X7R X8R	± 10 % ± 12.5 %	Leave the capacitors in ambient condition for 6 to 24h (Class1) or 24 2h (Class2) before measurement.	
		Q (Class1)	-	ited citance	Q	ZII (Class2) selote measarement.	
			30pF ar	nd over	350 min.		
			10pF ar to unde		275+5/2×C min.		
			Unde	r 10pF	200+10×C min.		
			C : R	ated ca	pacitance (pF)		
		D. F. (Class2)	200% of initial spec. max. $1,000M\Omega \text{ min.}$ (As for the capacitors of rated voltage 16, 10, 6.3V DC, $10M\Omega \cdot \mu F$ min.,)				
		Insulation Resistance					
14	Moisture Resistance	External appearance	No mechanical damage.			Reflow solder the capacitors on a P.C.Board shown in Appendix 1 to 3	
		Capacitance	Charact	eristics	Change from the value before test	before testing. Apply the rated voltage at	
			Class1	C H C0G	±7.5% or ±0.75pF, whichever larger.	temperature 40 ± 2°C and 90 to 95%RH for 500 +24,0h.	
			Class2	J B X5R X7R X8R	± 10 % ± 12.5 %	Charge/discharge current shall not exceed 50mA.	
						Leave the capacitors in ambient condition for 6 to 24h (Class1) or 24	
		Q (Class1)	Rate Capaci		Q	2h (Class2) before measurement.	
			30pF and	dover	200 min.	Voltage conditioning (only for class 2 Voltage treat the capacitors under	
			Under	30pF	100+10/3×C min.	testing temperature and voltage for 1	
			C : Rated capacitance (pF)			hour. Leave the capacitors in ambient	
		D. F. (Class2)	200% of ir	nitial sp	ec. max.	condition for 24±2h before measurement.	
		Insulation Resistance	(As for the	500MΩ or min. (As for the capacitors of rated voltage 16, 10, 6.3V DC, $5M\Omega \cdot \mu F$ min.,)		Use this measurement for initial value.	

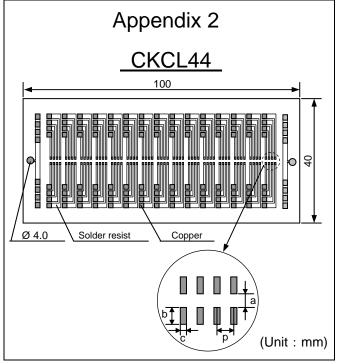


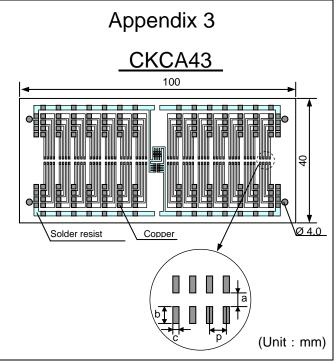
No.	Item		Performance			Test or inspection method
15	Life	External appearance	No mechanical damage.		lamage.	Reflow solder the capacitors on a P.C.Board shown in Appendix 1 to 3 before testing.
		Capacitance	Charact Class1	СН	Change from the value before test ±3% or ±0.3pF,	Below the voltage shall be applied at maximum operating temperature ± 2°C for 1,000 +48, 0h.
			Class2	J B X5R X7R X8R	± 12.5 % ± 15 %	Applied voltage Rated voltage × 2 Rated voltage × 1.5
		Q (Class1)		ited citance	Q	Rated voltage × 1 For information which product has
			30pF a	nd over	350 min.	which applied voltage, please contact
			10pF a to unde		275+5/2×C min.	with our sales representative. Charge/discharge current shall not
			Unde	r 10pF	200+10×C min.	exceed 50mA. Leave the capacitors in ambient
			C : Rated capacitance (pF)		itance (pF)	condition for 6 to 24h (Class1) or 24±2h (Class2) before measurement.
		D. F. (Class2)	200% of initial spec. max.			Voltage conditioning (only for class 2) Voltage treat the capacitors under testing temperature and voltage for 1 hour. Leave the capacitors in ambient condition for 24±2h before measurement. Use this measurement for initial value.
		Insulation Resistance		1,000MΩ or min. (As for the capacitors of rated voltage 16, 10, 6.3V DC, $10MΩ·μF$ min.,)		

^{*}As for the initial measurement of capacitors (Class2) on number 8,11,12 and 13, leave capacitors at 150 -10,0°C for 1 hour and measure the value after leaving capacitors for 24 \pm 2h in ambient condition.









Material : Glass Epoxy (As per JIS C6484 GE4)

P.C. Board thickness: 1.6mm

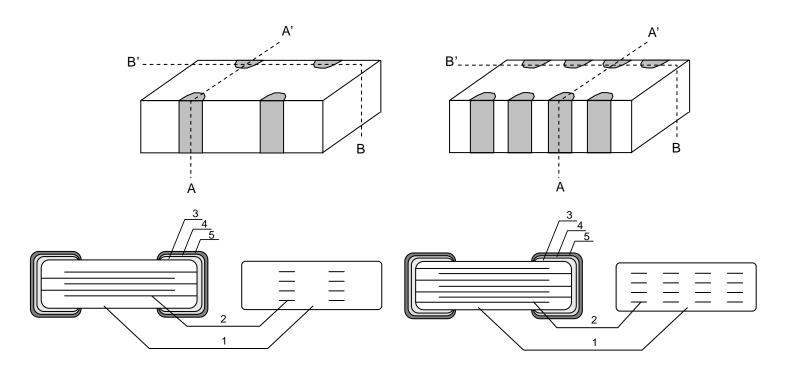
Copper (thickness 0.035mm)

Solder resist

TDV (FIA atula)	Dimensions (mm)					
TDK (EIA style)	а	b	С	р		
CKCM25	0.5	0.5	0.36	0.64		
CKCL22	0.6	0.6	0.45	1.0		
CKCL44	0.6	0.7	0.2	0.5		
CKCA43	1.0	0.7	0.3	8.0		

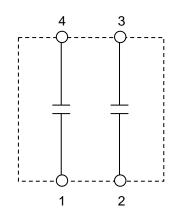


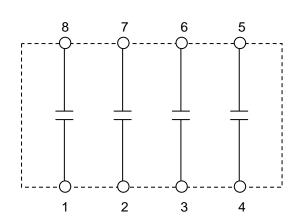
8. INSIDE STRUCTURE AND MATERIAL



No.	NAME	MATERIAL			
NO.	NAME	Class1	Class2		
1	Dielectric	CaZrO₃	BaTiO ₃		
2	Electrode	Nickel (Ni)			
3		Copper (Cu)			
4	Termination	Nickel (Ni)			
5		Tin (Sn)			

9. EQUIVALENT CIRCUIT





10. Caution

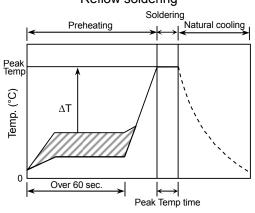
	I					
No.	Process	Condition				
1	Operating Condition (Storage,	 Storage The capacitors must be stored in an ambient temperature of 5 to 40°C with a relative humidity of 20 to 70%RH. The products should be used within 6 months upon receipt. 				
	 The capacitors must be operated and stored in an environment free of dew condensation and these gases such as Hydrogen Sulphide, Hydrogen Sulphate, Chlorine, Ammonia and sulfur. 					
		3) Avoid storing in sun light and falling of dew.				
		4) Do not use capacitors under high humidity and high and low atmospheric pressure which may affect capacitors reliability.				
		5) Capacitors should be tested for the solderability when they are stored for long time.				
		1-2. Handling in transportation				
		In case of the transportation of the capacitors, the performance of the capacitors may be deteriorated depending on the transportation condition. (Refer to JEITA RCR-2335B 9.2 Handling in transportation)				
2	Circuit design A Caution	2-1. Operating temperature Operating temperature should be followed strictly within this specification, especiall be careful with maximum temperature. 1) Do not use capacitors above the maximum allowable operating temperature.				
		2) Surface temperature including self heating should be below maximum operating				
		temperature. (Due to dielectric loss, capacitors will heat itself when AC is applied. Especially at high frequencies around its SRF, the heat might be so extreme that it may damage itself or the product mounted on. Please design the circuit so that the maximum temperature of the capacitors including the self heating to be below the maximum allowable operating temperature. Temperature rise at capacitor surface shall be below 20°C)				
		 The electrical characteristics of the capacitors will vary depending on the temperature. The capacitors should be selected and designed in taking the temperature into consideration. Operating voltage Operating voltage across the terminals should be below the rated voltage. When AC and DC are super imposed, V_{0-P} must be below the rated voltage. 				
		AC or pulse with overshooting, V_{P-P} must be below the rated voltage. (1) and (2)				
		When the voltage is started to apply to the circuit or it is stopped applying, the irregular voltage may be generated for a transit period because of resonance or switching. Be sure to use the capacitors within rated voltage containing these Irregular voltage.				
		Voltage (1) DC voltage (2) DC+AC voltage (3) AC voltage				
		Positional Measurement (Rated voltage) 0 V _{0-P} 0 V _{P-P} 0				
		Voltage (4) Pulse voltage (A) (5) Pulse voltage (B)				
		Positional Measurement (Rated voltage)				

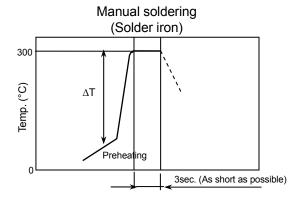
No.	Process			Condition		
2	Circuit design A Caution		f repetitive high hay be reduced.	frequency AC or	pulse is applied,	
	_	3) The effective capacitance will vary depending on applied DC and AC voltage The capacitors should be selected and designed in taking the voltages into consideration.				
			pacitors (Class 2) ay vibrate themse		and/or pulse voltaç te audible sound.	ges, the
3[Designing P.C.board	and the more	e amount of solde likely that it will br	er, the higher the eak. When desig	t effect on the reliant stress on the chipning a P.C.board, er amount of solde	capacitors, determine the
		Avoid using common solder land for multiple terminations and provide individual solder land for each terminations.				
		3) Size and recommended land dimensions.				
			A B C			
						(mm)
		Type Symbol	CKCM25	CKCL22	CKCL44	CKCA43
		P	0.64	1.0	0.5	0.8
		A	0.3	0.4	0.55	0.6 - 0.7
		В	0.45	0.6	0.6	0.8 - 1.0
		С	0.3	0.5	0.25	0.4

No.	Process			Condition			
3	Designing P.C.board	4)	Recommended chip capacitors layout is as following.				
		_		Disadvantage against bending stress	Advantage against bending stress		
			Mounting face	Perforation or slit	Perforation or slit		
				Break P.C.board with mounted side up.	Break P.C.board with mounted side down.		
		II.	Chip arrangement (Direction)	Mount perpendicularly to perforation or slit Perforation or slit	Mount in parallel with perforation or slit Perforation or slit		
		_		Closer to elit in higher etrope	Away from alit in loss atrass		
		_	Distance from slit	Closer to slit is higher stress $(\ell_1 < \ell_2)$	Away from slit is less stress		

No.	Process	Condition
3	Designing P.C.board	5) Mechanical stress varies according to location of chip capacitors on the P.C.board.
		Perforation
		A Slit B
		The stress in capacitors is in the following order. A > B = C > D > E
4	Mounting	 4-1. Stress from mounting head If the mounting head is adjusted too low, it may induce excessive stress in the chip capacitors to result in cracking. Please take following precautions. 1) Adjust the bottom dead center of the mounting head to reach on the P.C.board surface and not press it. 2) Adjust the mounting head pressure to be 1 to 3N of static weight. 3) To minimize the impact energy from mounting head, it is important to provide support from the bottom side of the P.C.board. See following examples.
		Not recommended Recommended
		Single sided mounting Support
		Double-sides mounting Solder peeling Crack Support
		When the centering jaw is worn out, it may give mechanical impact on the capacitors to cause crack. Please control the close up dimension of the centering jaw and provide sufficient preventive maintenance and replacement of it.

No.	Process	Condition
5	Soldering	5-1. Flux selection Although highly-activated flux gives better solderability, substances which increase activity may also degrade the insulation of the chip capacitors. To avoid such degradation, it is recommended following.
		It is recommended to use a mildly activated rosin flux (less than 0.1wt% chlorine). Strong flux is not recommended.
		Excessive flux must be avoided. Please provide proper amount of flux.
		3) When water-soluble flux is used, enough washing is necessary.
		5-2. Recommended soldering profile by various methods
		Reflow soldering





5-3. Recommended soldering peak temp and peak temp duration

Temp./Duration	Reflow soldering		
Solder	Peak temp(°C)	Duration(sec.)	
Sn-Pb Solder	230 max.	20 max.	
Lead Free Solder	260 max.	10 max.	

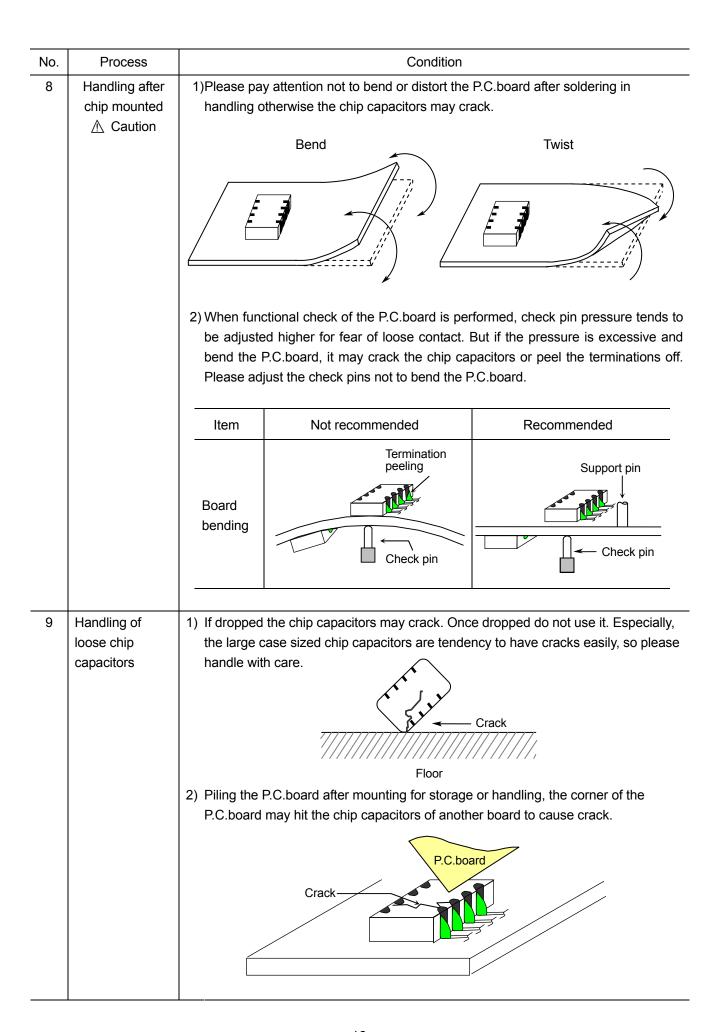
Recommended solder compositions Sn-37Pb (Sn-Pb solder) Sn-3.0Ag-0.5Cu (Lead Free Solder)



No.	Process			Cond	ition		
5	Soldering		iding thermal shoc	k			
		1) Preh					
			Soldering	01/01/05 01/0	Temp. (°C)	01/04/0	
				CKCM25, CKC	L22, CKCL44	CKCA43	
			Reflow soldering	ΔT ≤ °	150	ΔT ≤ 130	
			Manual soldering	ΔT ≤ 1	150	ΔT ≤ 130	
		Natu clea 5-5. Ame to	ning, the temperatount of solder Excessive solder w	ure difference (∆T ill induce higher te es and it may resu) must be less that nsile force in chip It in chip cracking		
		Exc	cessive der	g G G G G G G G G G G G G G G G G G G G	₹	her tensile force in capacitors to cause ck	
		Ade	equate		Maximum amo		
		Ins	ufficient der		cau chir	v robustness may use contact failure or o capacitors come off P.C.board.	
		F C C-1	d i - b a l d -				
			der repair by solde ection of the solderi				
		Tip lan hea	temperature of so d size. The higher at shock may cause	lder iron varies by the tip temperature e a crack in the ch	e, the quicker the ip capacitors.	d material and solder operation. However,	
		tim	Please make sure the tip temp. before soldering and keep the peak temp a time in accordance with following recommended condition. (Please preheat chip capacitors with the condition in 5-4 to avoid the thermal shock.)				
		Re	ecommended solde	er iron condition (S	n-Pb Solder and	Lead Free Solder)	
			Temp. (°C)	Duration (sec.)	Wattage (W)	Shape (mm)	
			300 max.	3 max.	20 max.	Ø 3.0 max.	
		,	se crack. Do not to	•		of chip capacitors may erminations by solder	

No.	Process	Condition			
5-7. Sn-Zn solder Sn-Zn solder affects product reliability. Please contact TDK in advance when utilize Sn-Zn solder. 5-8. Countermeasure for tombstone The misalignment between the mounted positions of the capacitors and the patterns should be minimized. The tombstone phenomenon may occur the capacitors are mounted (in longitudinal direction) in the same direction of soldering. (Refer to JEITA RCR-2335B Annex 1 (Informative) Recommendations to tombstone phenomenon)					
6	Cleaning	 If an unsuitable cleaning fluid is used, flux residue or some foreign articles may stick to chip capacitors surface to deteriorate especially the insulation resistance. If cleaning condition is not suitable, it may damage the chip capacitors. Insufficient washing Terminal electrodes may corrode by Halogen in the flux. Halogen in the flux may adhere on the surface of capacitors, and lower the insulation resistance. Water soluble flux has higher tendency to have above mentioned 			
		problems (1) and (2).			
		2)-2. Excessive washing			
		When ultrasonic cleaning is used, excessively high ultrasonic energy output can affect the connection between the ceramic chip capacitor's body and the terminal electrode. To avoid this, following is the recommended condition.			
		Power: 20 W/ & max. Frequency: 40 kHz max. Washing time: 5 minutes max.			
		2)-3. If the cleaning fluid is contaminated, density of Halogen increases, and it may bring the same result as insufficient cleaning.			
7	Coating and molding of the P.C.board	 When the P.C.board is coated, please verify the quality influence on the product. Please verify carefully that there is no harmful decomposing or reaction gas emission during curing which may damage the chip capacitors. Please verify the curing temperature. 			





No.	Process	Condition
10	Capacitance aging	The capacitors (Class 2) have aging in the capacitance. They may not be used in precision time constant circuit. In case of the time constant circuit, the evaluation should be done well.
11	Estimated life and estimated failure rate of capacitors	As per the estimated life and the estimated failure rate depend on the temperature and the voltage. This can be calculated by the equation described in JEITA RCR-2335B Annex 6 (Informative) Calculation of the estimated lifetime and the estimated failure rate (Voltage acceleration coefficient: 3 multiplication rule, Temperature acceleration coefficient: 10°C rule) The failure rate can be decreased by reducing the temperature and the voltage but they will not be guaranteed.
12	Others Caution	The products listed on this specification sheet are intended for use in general electronic equipment (AV equipment, telecommunications equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment, industrial robots) under a normal operation and use condition.
		The products are not designed or warranted to meet the requirements of the applications listed below, whose performance and/or quality require a more stringent level of safety or reliability, or whose failure, malfunction or trouble could cause serious damage to society, person or property. Please understand that we are not responsible for any damage or liability caused by use of the products in any of the applications below or for any other use exceeding the range or conditions set forth in this specification sheet. If you intend to use the products in the applications listed below or if you have special requirements exceeding the range or conditions set forth in this specification, please contact us.
		 (1) Aerospace/Aviation equipment (2) Transportation equipment (cars, electric trains, ships, etc.) (3) Medical equipment (4) Power-generation control equipment (5) Atomic energy-related equipment (6) Seabed equipment (7) Transportation control equipment (8) Public information-processing equipment (9) Military equipment (10) Electric heating apparatus, burning equipment (11) Disaster prevention/crime prevention equipment (12) Safety equipment (13) Other applications that are not considered general-purpose applications When designing your equipment even for general-purpose applications, you are kindly requested to take into consideration securing protection circuit/device or providing backup circuits in your equipment.



11. Packaging label

Packaging shall be done to protect the components from the damage during transportation and storing, and a label which has the following information shall be attached.

- 1) Inspection No.
- 2) TDK P/N
- 3) Customer's P/N
- 4) Quantity

*Composition of Inspection No.

Example
$$\underline{M}$$
 $\underline{2}$ \underline{A} - \underline{OO} - \underline{OOO} (a) (b) (c) (d) (e)

- a) Line code
- b) Last digit of the year
- c) Month and A for January and B for February and so on. (Skip I)
- d) Inspection Date of the month.
- e) Serial No. of the day

12. Bulk packaging quantity

Total number of components in a plastic bag for bulk packaging: 1,000pcs.

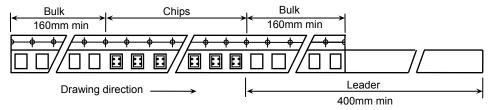
13. TAPE PACKAGING SPECIFICATION

1. CONSTRUCTION AND DIMENSION OF TAPING

1-1. Dimensions of carrier tape

Dimensions of paper tape shall be according to Appendix 4. Dimensions of plastic tape shall be according to Appendix 5.

1-2. Bulk part and leader of taping

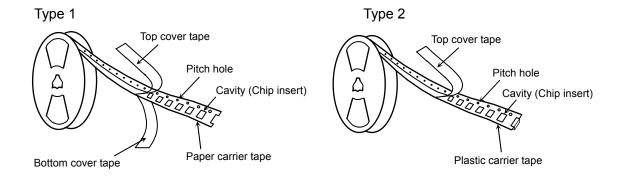


1-3. Dimensions of reel

Dimensions of Ø178 reel shall be according to Appendix 6.

Dimensions of Ø330 reel shall be according to Appendix 7.

1-4. Structure of taping

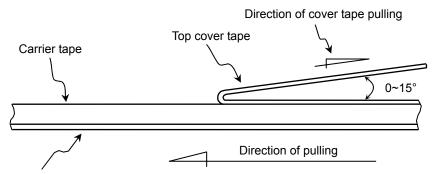


2. CHIP QUANTITY

Typo	Taping	Chip quantity (pcs.)			
Туре	Material	φ178mm reel	φ330mm reel		
CKCM25	Paper				
CKCL22	Plastic	4,000	10.000		
CKCL44	Paper		10,000		
CKCA43	Plastic	2,000			

3. PERFORMANCE SPECIFICATIONS

3-1. Fixing peeling strength (top tape) 0.05-0.7N. (See the following figure.)



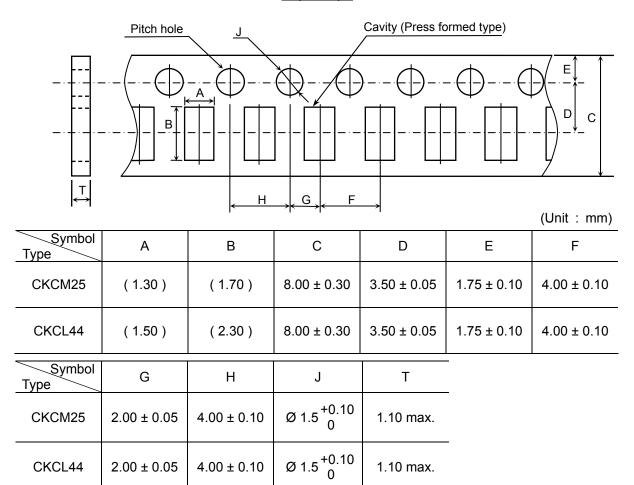
Bottom cover tape (Paper carrier tape of type 1)

- 3-2. Carrier tape shall be flexible enough to be wound around a minimum radius of 30mm with components in tape.
- 3-3. The missing of components shall be less than 0.1%
- 3-4. Components shall not stick to fixing tape.
- 3-5. The fixing tapes shall not protrude beyond the edges of the carrier tape not shall cover the sprocket holes.



Appendix 4

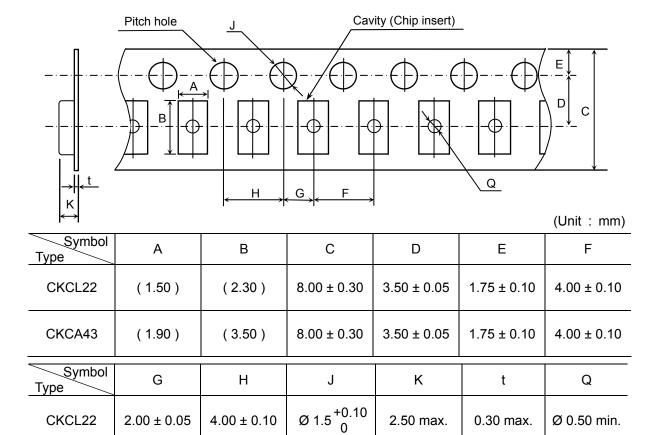
Paper Tape



^{*} The values in the parentheses () are for reference.

Appendix 5

Plastic Tape



Ø $1.5^{+0.10}_{0}$

2.50 max.

0.30 max.

Ø 0.50 min.

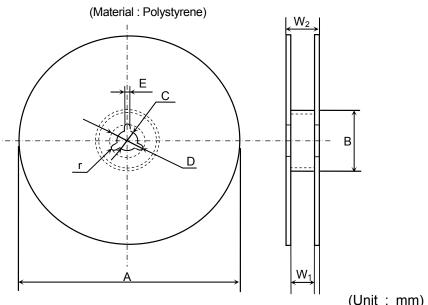
 4.00 ± 0.10

CKCA43

 2.00 ± 0.05

^{*} The values in the parentheses () are for reference.

Appendix 6

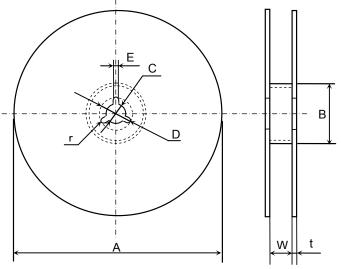


					ζ.	O
Symbol	А	В	С	D	E	W ₁
Dimension	Ø178 ± 2.0	Ø60 ± 2.0	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	9.0 ± 0.3

Symbol	W ₂	r
Dimension	13.0 ± 1.4	1.0

Appendix 7

(Material : Polystyrene)



(Unit : mm)

Symbol	А	В	С	D	E	W
Dimension	Ø382 max. (Nominal Ø330)	Ø50 min.	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	10.0 ± 1.5

Symbol	t	r	
Dimension	2.0 ± 0.5	1.0	