MOS FET

### FK6K02010L

## **Panasonic**

### FK6K02010L

### Silicon N-channel MOS FET

### For switching

#### ■ Features

- Low drain-source On-state Resistance:RDS(on)typ. = 13 m $\Omega$  (VGS = 4.5 V)
- · Low drive voltage: 2.5 V drive
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL : Level 1 compliant)
- Marking Symbol : TA

#### ■ Packaging

Embossed type (Thermo-compression sealing): 3 000 pcs / reel (standard)

■ Absolute Maximum Ratings Ta = 25 °C

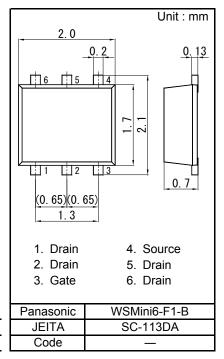
Parameter	Symbol	Rating	Unit
Drain-source surrender voltage	VDSS	20	V
Gate-source surrender voltage	VGSS	±10	V
Drain current	ID	4.5	Α
Peak drain current *1	IDp	18	Α
Power dissipation *2	PD	700	mW
Channel temperature	Tch	150	°C
Operating ambient temperature	Topr	-40 to +85	°C
Storage temperature	Tstg	-55 to +150	°C

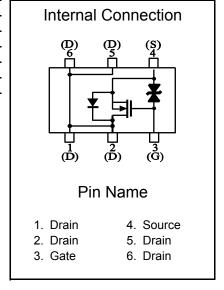
Note) \*1  $t = 10 \mu s$ , Duty Cycle < 1%

Established: 2010-06-07

: 2013-07-01

Revised





<sup>\*2</sup> Measuring on Glass epoxy board ( $25.4 \times 25.4 \times t0.8 \text{ mm}$ ) coated with copper foil, which has more than 300 mm<sup>2</sup> Absolute maximum rating without heat sink for PD is 150 mW.

Doc No. TT4-EA-12566 Revision. 2

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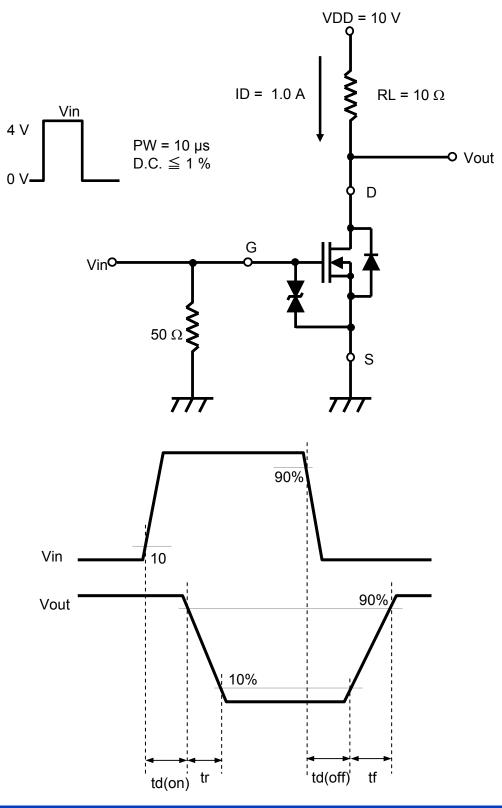
### ■ Electrical Characteristics Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Drain-source surrender voltage	VDSS	ID = 1 mA, VGS = 0	20			V
Drain-source cutoff current	IDSS	VDS = 20 V, VGS = 0			1.0	μA
Gate-source cutoff current	IGSS	$VGS = \pm 8 \text{ V}, VDS = 0$			±10	μA
Gate threshold voltage	Vth	ID = 1.0 mA, VDS = 10.0 V	0.4	0.85	1.3	V
Drain-source ON resistance	RDS(ON)1	ID = 2.0 A, VGS = 4.5 V		13	17.5	mΩ
	RDS(ON)2	ID = 1.0 A, VGS = 2.5 V		16	28	
Forward transfer admittance	Yfs	ID = 1.0 A, VDS =10 V	3.0			S
Short-circuit input capacitance (Common source)	Ciss			1 730		pF
Short-circuit output capacitance (Common source)	Coss	VDS = 10 V, VGS = 0, f = 1 MHz		155		pF
Reverse transfer capacitance (Common source)	Crss			150		pF
Turn-on delay time *1	td(on)	VDD = 10 V		19		ns
Rise time *1	tr	VGS = 0 to 4 V		30		ns
Turn-off delay time *1	td(off)	ID=1.0A		150		ns
Fall time *1	tf	1.00		75		ns

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

<sup>2. \*1</sup> Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time

\*1 Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time

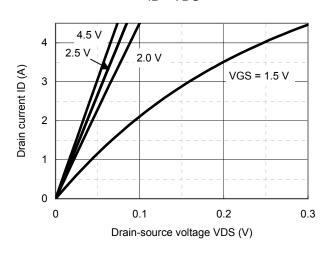


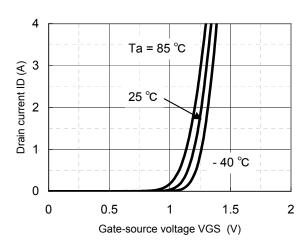
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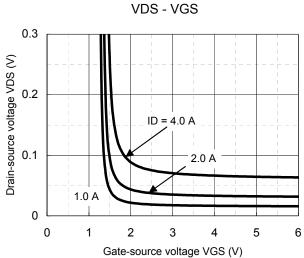
### Technical Data (reference)

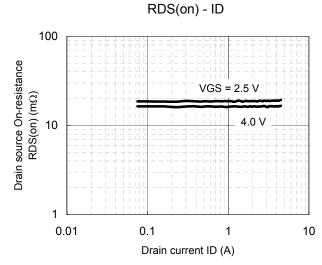
ID - VDS

ID - VGS

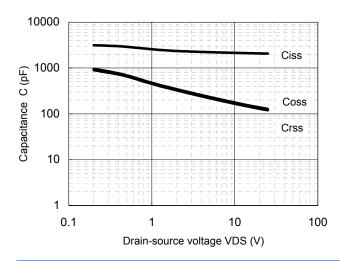








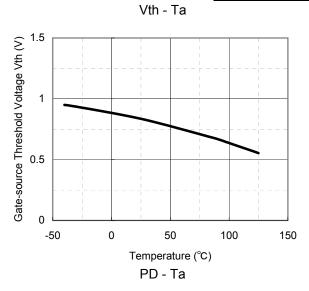
Capacitance - VDS

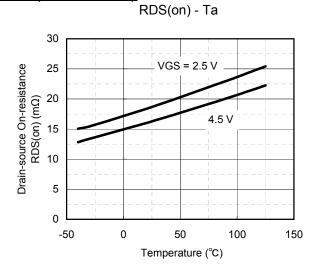


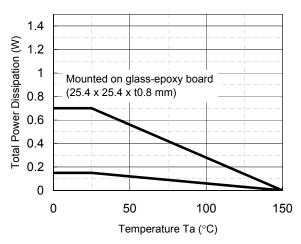
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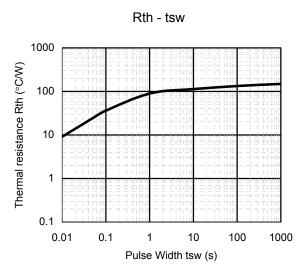
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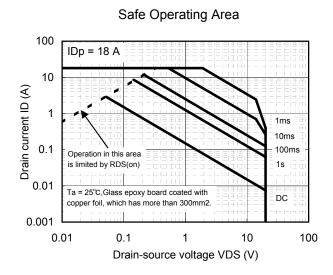
### Technical Data (reference)











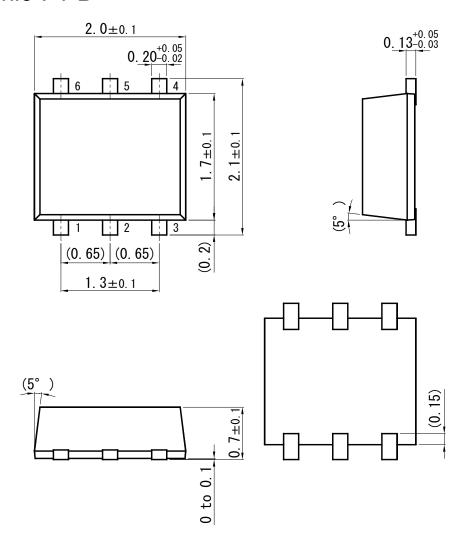
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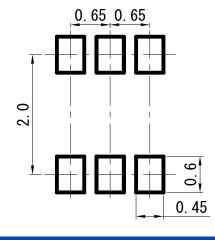
## FK6K02010L

WSMini6-F1-B

Unit: mm



■Land Pattern (Reference) (Unit : mm)



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