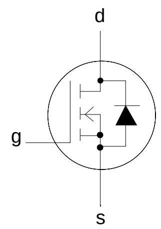
N-channel TrenchMOS™ transistor PHX23NQ10T

FEATURES

- **'Trench'** technology
- Low on-state resistance
- Fast switching

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 100 V

I_D = 13 A

$R_{DS(ON)} \leq 70$ mΩ

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full pack envelope using '**trench**' technology.

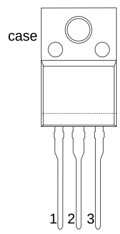
Applications:-
- d.c. to d.c. converters
- switched mode power supplies
- T.V. and computer monitor power supplies

The PHX23NQ10T is supplied in the SOT186A (FPAK) conventional leaded package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

SOT186A (FPAK)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 ˚C to 150˚C	-	100	V
V_{DGR}	Drain-gate voltage	T_j = 25 ˚C to 150˚C; R_{GS} = 20 kΩ	-	100	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Continuous drain current	T_{mb} = 25 ˚C; V_{GS} = 10 V	-	13	A
		T_{mb} = 100 ˚C; V_{GS} = 10 V	-	8	A
I_{DM}	Pulsed drain current	T_{mb} = 25 ˚C	-	52	A
P_D	Total power dissipation	T_{mb} = 25 ˚C	-	27	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	150	˚C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_{AS} = 14 A; t_p = 100 µs; T_j prior to avalanche = 25˚C; $V_{DD} \leq$ 25 V; R_{GS} = 50 Ω; V_{GS} = 10 V; refer to fig:15	-	93	mJ
I_{AS}	Peak non-repetitive avalanche current		-	23	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	4.6	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	SOT186a package, in free air	-	55	-	K/W

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	100	-	-	V
		T_j = -55˚C	89	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2	3	4	V
		T_j = 150˚C	1.25	-	-	V
		T_j = -55˚C	-	-	6	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 13 A	-	49	70	mΩ
		T_j = 150˚C	-	115	163	mΩ
I_{GSS}	Gate source leakage current	V_{GS} = ± 10 V; V_{DS} = 0 V	-	10	100	nA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V	-	0.05	10	µA
		T_j = 150˚C	-	-	500	µA
$Q_{g(tot)}$	Total gate charge	I_D = 23 A; V_{DD} = 80 V; V_{GS} = 10 V	-	22	-	nC
Q_{gs}	Gate-source charge		-	5	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	10	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 50 V; R_D = 2.2 Ω;	-	8	-	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 5.6 Ω	-	39	-	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	26	-	ns
t_f	Turn-off fall time		-	24	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	890	1187	pF
C_{oss}	Output capacitance		-	139	167	pF
C_{rss}	Feedback capacitance		-	83	109	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	13	A
I_{SM}	Pulsed source current (body diode)		-	-	92	A
V_{SD}	Diode forward voltage	I_F = 11 A; V_{GS} = 0 V	-	0.9	1.2	V
t_{rr}	Reverse recovery time	I_F = 11 A; -dI_F/dt = 100 A/µs;	-	64	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 25 V	-	120	-	nC

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

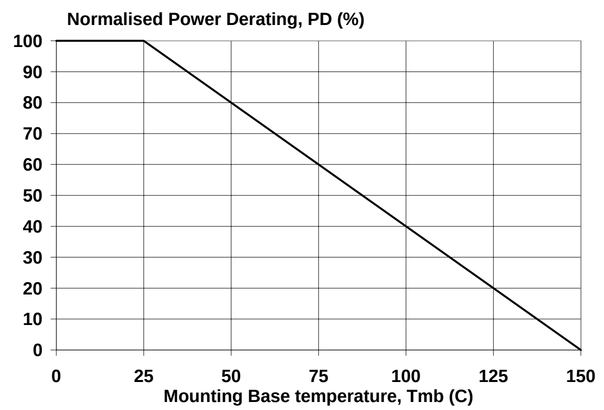


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D/P_{D\ 25\ ^\circ C} = f(T_{mb})$

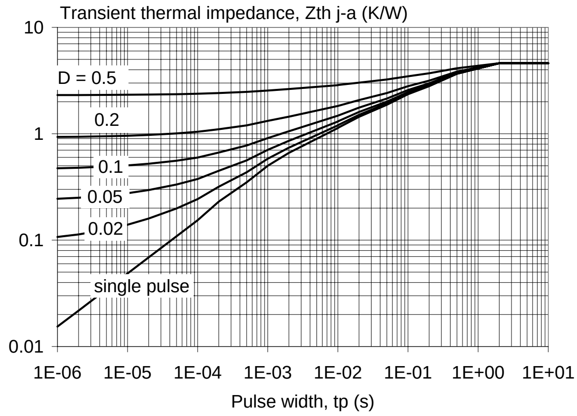


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

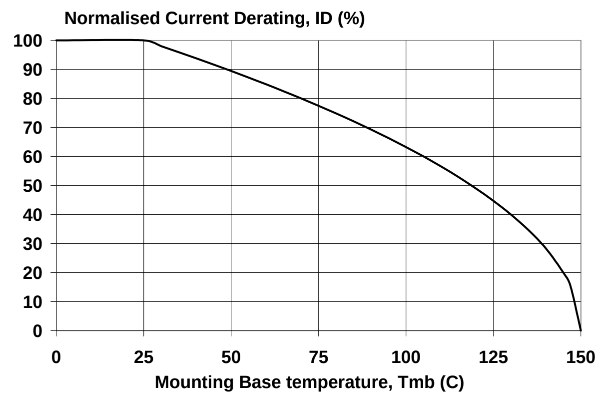


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D/I_{D\ 25\ ^\circ C} = f(T_{mb})$; conditions: $V_{GS} \geq 10$ V

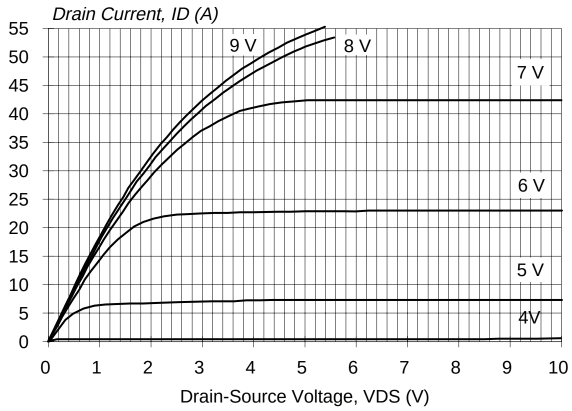


Fig.5. Typical output characteristics, $T_j = 25\ ^\circ C$.
$I_D = f(V_{DS})$

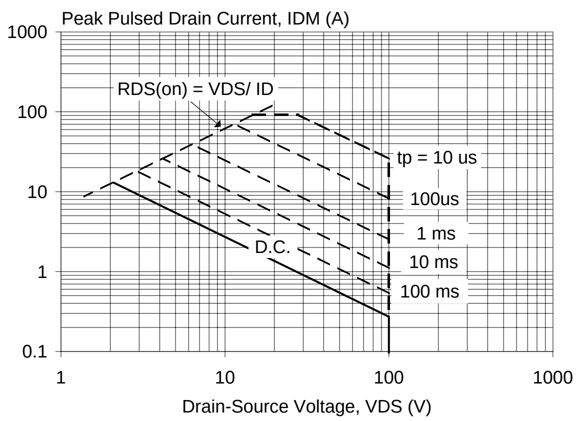


Fig.3. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

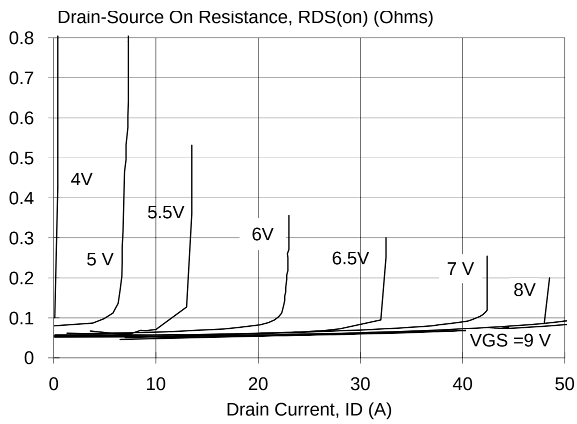


Fig.6. Typical on-state resistance, $T_j = 25\ ^\circ C$.
$R_{DS(ON)} = f(I_D)$

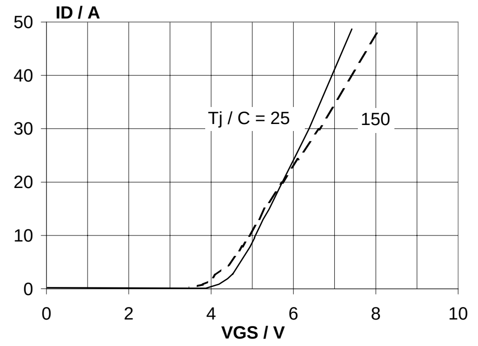


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$

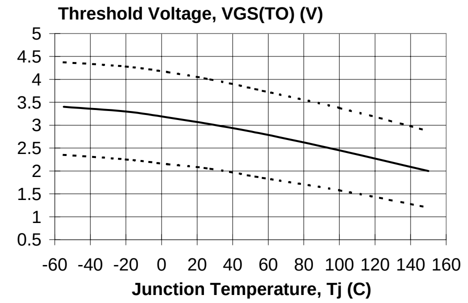


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1$ mA; $V_{DS} = V_{GS}$

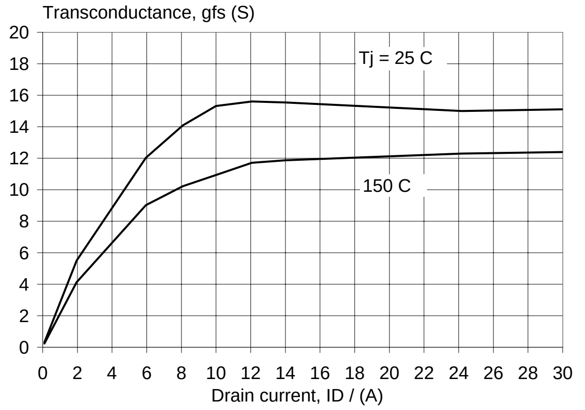


Fig.8. Typical transconductance, $T_j = 25\ ^\circ C$.
$g_{fs} = f(I_D)$

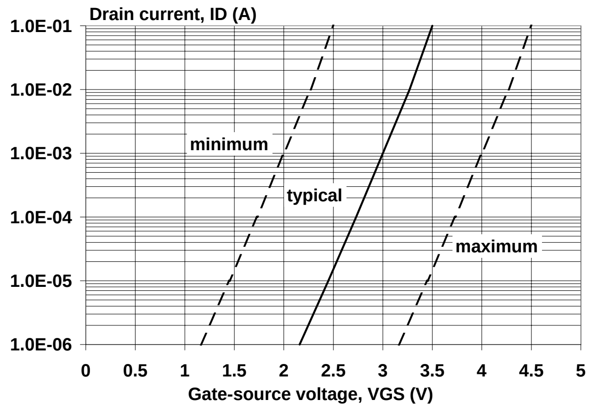


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25\ ^\circ C$; $V_{DS} = V_{GS}$

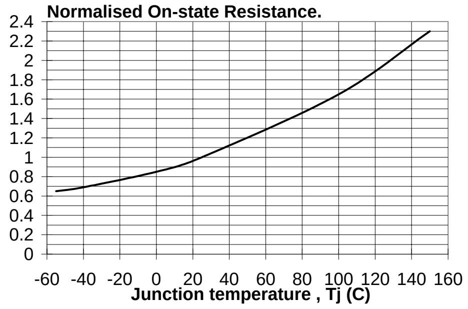


Fig.9. Normalised drain-source on-state resistance.
$R_{DS(ON)}/R_{DS(ON)25\ ^\circ C} = f(T_j)$

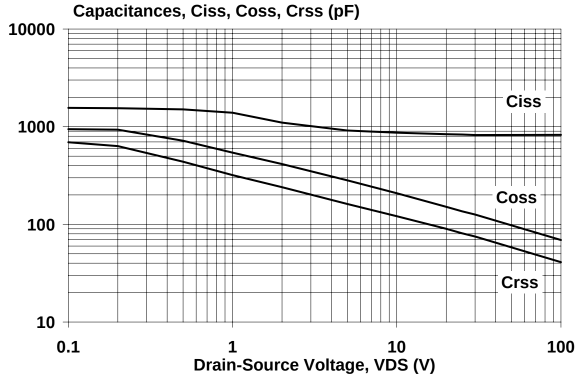


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

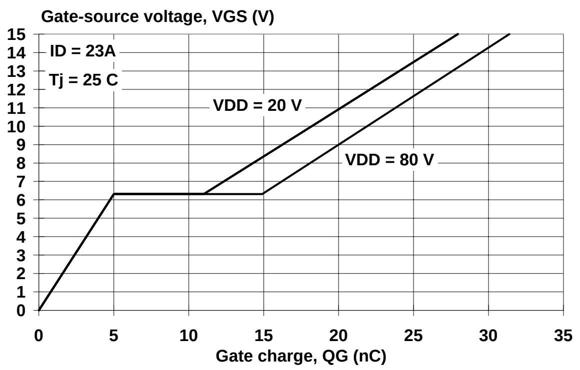


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$

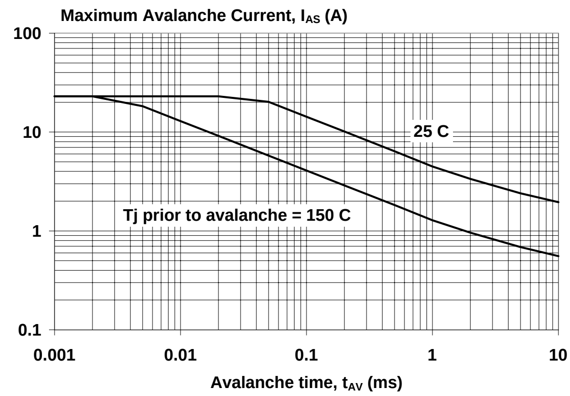


Fig.15. Maximum permissible non-repetitive avalanche current (I_{AS}) versus avalanche time (t_{AV}); unclamped inductive load

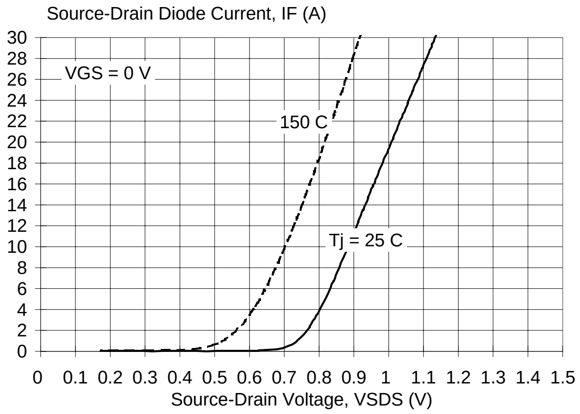


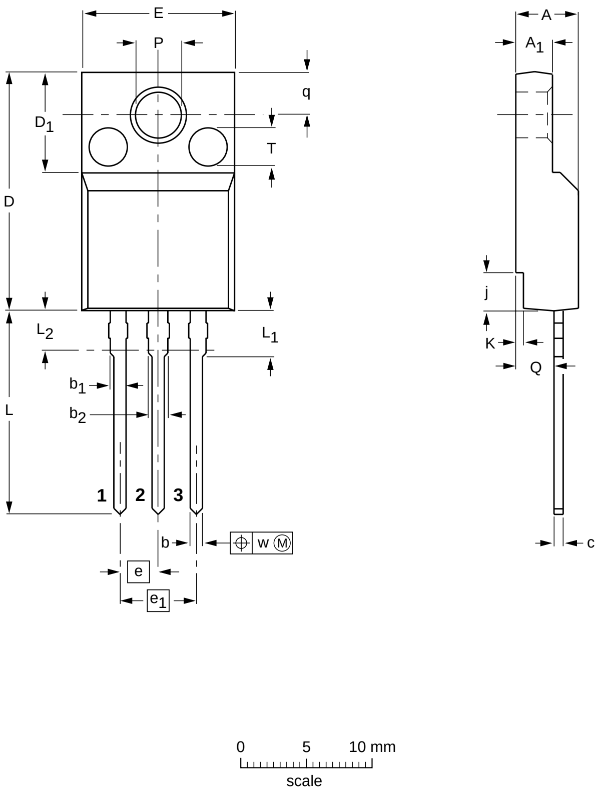
Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 lead TO-220 **SOT186A**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j	K	L	L_1	L_2 (1) max.	P	Q	q	T (2)	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.2	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 2.3	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

Notes

1. Terminal dimensions within this zone are uncontrolled. Terminals in this zone are not tinned.
2. Both recesses are ∅ 2.5 × 0.8 max. depth

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT186A		TO-220				97-06-11

Fig.16. SOT186A; The seating plane is electrically isolated from all terminals.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for F-pack envelopes.
3. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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