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Kind regards,

Team Nexperia

DISCRETE SEMICONDUCTORS



Product specification Supersedes data of 1997 Jun 23 2001 May 18



Product specification

N-channel enhancement mode vertical D-MOS transistor

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 package, intended for use as a surface-mounted device in line current interrupters in telephone sets and for application in relay, high speed and line transformer drivers.

PINNING - SOT223

PIN	PIN DESCRIPTION		
	Code: BSP89		
1	gate		
2	drain		
3	source		
4	drain		

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT	
V _{DS}	drain-source voltage (DC) 240 V			
V _{GSth}	gate-source threshold voltage 2 V			
ID	drain current (DC) 375 m		mA	
R _{DSon}	drain-source on-state resistance 5 Ω		Ω	



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DS}	drain-source voltage (DC)		_	240	V
V _{GSO}	gate-source voltage (DC)	open drain	-	±20	V
I _D	drain current (DC)		_	375	mA
I _{DM}	peak drain current		-	1.5	А
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	_	1.5	W
T _{stg}	storage temperature		-55	+150	°C
Tj	junction temperature		-	150	°C

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm².

BSP89

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient; note 1	83.3	K/W

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm².

CHARACTERISTICS

 $T_i = 25 \ ^{\circ}C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	drain-source breakdown voltage	$I_D = 10 \ \mu A; V_{GS} = 0$	240	-	-	V
I _{DSS}	drain-source leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0$	_	-	200	nA
I _{GSS}	gate-source leakage current	$V_{GS} = \pm 20 \text{ V}; V_{DS} = 0$	-	-	100	nA
V _{GSth}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{GS} = V_{DS}$	0.8	-	2	V
R _{DSon}	drain-source on-state resistance	I _D = 340 mA; V _{GS} = 10 V	_	2.8	5	Ω
		I _D = 340 mA; V _{GS} = 4.5 V	_	-	7.5	Ω
Y _{fs}	transfer admittance	I _D = 340 mA; V _{DS} = 25 V	140	600	-	mS
Ciss	input capacitance	$V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz$	_	100	120	pF
C _{oss}	output capacitance	V _{DS} = 25 V; V _{GS} = 0; f = 1 MHz	_	20	30	pF
C _{rss}	reverse transfer capacitance	$V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz$	-	10	15	pF
Switching ti	mes (see Figs 3 and 4)	· ·			·	
t _{on}	turn-on time	$I_D = 250 \text{ mA}; V_{DD} = 50 \text{ V};$ $V_{GS} = 0 \text{ to } 10 \text{ V}$	-	6	10	ns
t _{off}	turn-off time	$I_D = 250 \text{ mA}; V_{DD} = 50 \text{ V};$ $V_{GS} = 0 \text{ to } 10 \text{ V}$	-	47	60	ns





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PACKAGE OUTLINE



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DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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NOTES

Philips Semiconductors – a worldwide company

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB, Argentina: see South America Tel. +31 40 27 82785, Fax. +31 40 27 88399 Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140, New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND, Tel. +61 2 9704 8141, Fax. +61 2 9704 8139 Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 1 60 101 1248. Fax. +43 1 60 101 1210 Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6, 220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773 Belgium: see The Netherlands Brazil: see South America Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor, 51 James Bourchier Blvd., 1407 SOFIA, Tel. +359 2 68 9211, Fax. +359 2 68 9102 Canada: PHILIPS SEMICONDUCTORS/COMPONENTS, Tel. +1 800 234 7381, Fax. +1 800 943 0087 China/Hong Kong: 501 Hong Kong Industrial Technology Centre, 72 Tat Chee Avenue, Kowloon Tong, HONG KONG, Tel. +852 2319 7888, Fax. +852 2319 7700 Colombia: see South America Czech Republic: see Austria Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V, Tel. +45 33 29 3333, Fax. +45 33 29 3905 Finland: Sinikalliontie 3, FIN-02630 ESPOO, Tel. +358 9 615 800, Fax. +358 9 6158 0920 France: 7 - 9 Rue du Mont Valérien, BP317, 92156 SURESNES Cedex, Tel. +33 1 4728 6600, Fax. +33 1 4728 6638 Germany: Hammerbrookstraße 69, D-20097 HAMBURG, Tel. +49 40 2353 60, Fax. +49 40 2353 6300 Hungary: Philips Hungary Ltd., H-1119 Budapest, Fehervari ut 84/A, Tel: +36 1 382 1700, Fax: +36 1 382 1800 India: Philips INDIA Ltd, Band Box Building, 2nd floor, 254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025, Tel. +91 22 493 8541, Fax. +91 22 493 0966 Indonesia: PT Philips Development Corporation, Semiconductors Division. Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510, Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080 Ireland: Newstead, Clonskeagh, DUBLIN 14, Tel. +353 1 7640 000, Fax. +353 1 7640 200 Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053, TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007 Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI), Tel. +39 039 203 6838. Fax +39 039 203 6800 Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057 Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. +82 2 709 1412, Fax. +82 2 709 1415 Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR, Tel. +60 3 750 5214, Fax. +60 3 757 4880 Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,

Middle East: see Italy For all other countries apply to: Philips Semiconductors,

Marketing Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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