S1C17 Manual errata

ITEM: LCD Driver List of Output	ut Pins		
Object manuals	Document	Items	Pages
	codes		
S1C17M10Technical Manual	413180100	17.2.1 List of Output Pins	17-2
S1C17M30/M31/M32/M33/M34Tec	413495501	18.2.1 List of Output Pins	18-3
hnical Manual			
S1C17W13Technical Manual	413180301	18.2.1 List of Output Pins	18-2
S1C17W14/W16Technical Manual	412910200	16.2.1 List of Output Pins	18-2
S1C17W15Technical Manual	412645602	17.2.1 List of Output Pins	17-2
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S1C17W34/W35/W36Technical	440007404	18.2.1 List of Output Pins	18-2
Manual	413237401		
S7C17M11Technical Manual	413393800	17.2.1 List of Output Pins	17-2
S1C17M10Technical Manual			

(Error)

The COM8-15 outputs and SEG87-80 outputs share the pins and selecting a drive duty switches the pins to COM pins or SEG pins. For the pin configuration, refer to "Drive Duty Switching."

Note: Be sure to avoid using the VC1 to VC5 pin outputs for driving external circuits.

(Correct)

The COM8-15 outputs and SEG87-80 outputs share the pins and selecting a drive duty switches the pins to COM pins or SEG pins. For the pin configuration, refer to "Drive Duty Switching."

Note:

- Be sure to avoid using the VC1 to VC5 pin outputs for driving external circuits.
- <u>When LCD panel is connected, LCD16CTL.LCDDIS bit should be set to 1. If it has been set to 0, there is a</u> possibility that LCD panel's characteristics is fluctuated.

S1C17M30/M31/M32/M33/M34 Technical Manual, S7C17M11 Technical Manual

(Error)

The COM4-7 outputs and SEG0-4 outputs share the pins and selecting a drive duty switches the pins to COM pins or SEG pins. For the pin configuration, refer to "Drive Duty Switching."

Note: Be sure to avoid using the VC1 to VC3 pin outputs of the model with an embedded LCD power supply for driving external circuits.

(Correct)

The COM4-7 outputs and SEG0-4 outputs share the pins and selecting a drive duty switches the pins to COM pins or SEG pins. For the pin configuration, refer to "Drive Duty Switching."

Note:

- Be sure to avoid using the VC1 to VC3 pin outputs of the model with an embedded LCD power supply for driving external circuits.
- <u>When LCD panel is connected, LCD8CTL.LCDDIS bit should be set to 1. If it has been set to 0, there is a</u> possibility that LCD panel's characteristics is fluctuated.

S1C17W13 Technical Manual

(Error)

If the port is shared with the LCD4A pin and other functions, the LCD4A output function must be assigned to the port before activating the LCD4A. For more information, refer to the "I/O Ports" chapter.

Note: Be sure to avoid using the VC1 to VC3 pin outputs for driving external circuits.

(Correct)

If the port is shared with the LCD4A pin and other functions, the LCD4A output function must be assigned to the port before activating the LCD4A. For more information, refer to the "I/O Ports" chapter.

Note:

- Be sure to avoid using the VC1 to VC3 pin outputs for driving external circuits.
- When LCD panel is connected, LCD4CTL.LCDDIS bit should be set to 1. If it has been set to 0, there is a possibility that LCD panel's characteristics is fluctuated.

S1C17W14/W16Technical Manual, S1C17W18Technical Manual

(Error)

The COM4-7 outputs and SEG0-4 outputs share the pins and selecting a drive duty switches the pins to COM pins or SEG pins. For the pin configuration, refer to "Drive Duty Switching."

Note: Be sure to avoid using the VC1 to VC3 pin outputs for driving external circuits

(Correct)

The COM4-7 outputs and SEG0-4 outputs share the pins and selecting a drive duty switches the pins to COM pins or SEG pins. For the pin configuration, refer to "Drive Duty Switching."

Note:

- Be sure to avoid using the VC1 to VC3 pin outputs for driving external circuits
- When LCD panel is connected, LCD8CTLLCDDIS bit should be set to 1. If it has been set to 0, there is a possibility that LCD panel's characteristics is fluctuated.

S1C17W15Technical Manual

(Error)

The COM4-7 outputs and SEG0-4 outputs share the pins and selecting a drive duty switches the pins to COM pins or SEG pins. For the pin configuration, refer to "Drive Duty Switching."

Note: Be sure to avoid using the VC1 to VC4 pin outputs for driving external circuits.

(Correct)

The COM4-7 outputs and SEG0-4 outputs share the pins and selecting a drive duty switches the pins to COM pins or SEG pins. For the pin configuration, refer to "Drive Duty Switching."

Note:

- Be sure to avoid using the VC1 to VC4 pin outputs for driving external circuits.
- When LCD panel is connected, LCD8CTLMODEN bit should be set to 1. If it has been set to 0, there is a possibility that LCD panel's characteristics is fluctuated.

S1C17W22/W23Technical Manual

(Error)

If the port is shared with the LCD24A pin and other functions, the LCD24A output function must be assigned to the port before activating the LCD24A. For more information, refer to the "I/O Ports" chapter.

Note: Be sure to avoid using the VC1 to VC4 pin outputs for driving external circuits.

(Correct)

f the port is shared with the LCD24A pin and other functions, the LCD24A output function must be assigned to the port before activating the LCD24A. For more information, refer to the "I/O Ports" chapter.

Note:

- Be sure to avoid using the VC1 to VC4 pin outputs for driving external circuits.
- When LCD panel is connected, LCD24CTLMODEN bit should be set to 1. If it has been set to 0, there is a possibility that LCD panel's characteristics is fluctuated.

S1C17W34/W35/W36Technical Manual

(Error)

The COM16-31 outputs and SEG0-15 or SEG79-64 outputs share the pins. Selecting a drive duty and COM[31:16] pin location switches the pins to COM pins or SEG pins. For the pin configuration, refer to "Drive Duty Switching."

Note: Be sure to avoid using the VC1 to VC5 pin outputs for driving external circuits.

(Correct)

The COM16-31 outputs and SEG0-15 or SEG79-64 outputs share the pins. Selecting a drive duty and COM[31:16] pin location switches the pins to COM pins or SEG pins. For the pin configuration, refer to "Drive Duty Switching."

Note:

- Be sure to avoid using the VC1 to VC5 pin outputs for driving external circuits.
- When LCD panel is connected, LCD32CTLMODEN bit should be set to 1. If it has been set to 0, there is a possibility that LCD panel's characteristics is fluctuated.

ITEM: LCD Driver List of Output	ut Pins		
Object manuals	Document codes	Items	Pages
S1C17M01Technical Manual	412361601	14.2.1 List of Output Pins	14-2
S1C17M10Technical Manual	413180100	17.2.1 List of Output Pins	17-2
S1C17M30/M31/M32/M33/M34Tec hnical Manual	413495501	18.2.1 List of Output Pins	18–3
S1C17W13Technical Manual	413180301	18.2.1 List of Output Pins	18-2
S1C17W14/W16Technical Manual	412910200	16.2.1 List of Output Pins	18-2
S1C17W15Technical Manual	412645602	17.2.1 List of Output Pins	17-2
S1C17W18Technical Manual	413129501	18.2.1 List of Output Pins	18-2
S1C17W22/W23Technical Manual	412690302	18.2.1 List of Output Pins	18-2
S1C17W34/W35/W36Technical Manual	413237401	18.2.1 List of Output Pins	18-2
S7C17M11Technical Manual	413393800	17.2.1 List of Output Pins	17-2

rror)				
		Table	14.2.1.1 L	ist of LCD8A Pins
Pin name	I/O	* Init	ial status*	Function
SEG31-0	0)	O (L)	Segment data output pin
COM7-0	0)	O (L)	Common data output pin
LFRO	0)	O (L)	Frame signal monitoring output pin
Vc1	Р		-	LCD panel drive power supply pin
Vc2	Р		-	LCD panel drive power supply pin
Vc3	Р		_	LCD panel drive power supply pin
CP1	A		-	LCD voltage booster capacitor connecting pin
CP2	А		-	LCD voltage booster capacitor connecting pin
Correct)				
				ist of LCD8A Pins
Pin name	I/C		ial status*	Function
SEG31-0	A		O (L)	Segment data output pin
COM7-0	A		0 (L)	Common data output pin
LFRO	0		0 (L)	Frame signal monitoring output pin
Vc1	P		-	LCD panel drive power supply pin
Vc2	P		-	LCD panel drive power supply pin
Vсз	P		-	LCD panel drive power supply pin
Vc3 CP1	P A		-	LCD panel drive power supply pin LCD voltage booster capacitor connecting pin
			-	LCD panel drive power supply pin
CP1	A		-	LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin
CP1 CP2 1C17M10 Technical M	A A Ianual	Table	- *	LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin Indicates the status when the pin is configured for LCD8A
CP1 CP2 1C17M10 Technical M Error) Pin name	A A Ianual	Table	- * 17.2.1.1 Lis	LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin Indicates the status when the pin is configured for LCD8A st of LCD16A Pins Function
CP1 CP2 1C17M10 Technical M Error) Pin name COM0-7	A A Ianual	Table Initial status*1 Hi-Z / O (L)*2	- * 17.2.1.1 Lis Common d	LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin Indicates the status when the pin is configured for LCD8A st of LCD16A Pins Function lata output pins
CP1 CP2 1C17M10 Technical M Error) Pin name COM0-7 COM8-15/SEG87-80	A A Ianual I/0*1 O O	Table Initial status ⁺¹ Hi-Z / O (L)+2 Hi-Z / O (L)+2	- * 17.2.1.1 Lis Common d General pu	LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin Indicates the status when the pin is configured for LCD8A st of LCD16A Pins Function lata output pins rpose IO/common data output/segment data output pins
CP1 CP2 1C17M10 Technical M Error) Pin name COM0-7 COM8-15/SEG87-80 SEG0-68	A A lanual I/0*1 0 0	Table Initial status ⁺¹ Hi-Z / O (L)+2 Hi-Z / O (L)+2 Hi-Z / O (L)+2	- * 17.2.1.1 Lis Common d General pu Segment d	LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin Indicates the status when the pin is configured for LCD8A st of LCD16A Pins Function lata output pins rpose IO/common data output/segment data output pins ata output pins
CP1 CP2 1C17M10 Technical M Error) Pin name COM0-7 COM8-15/SEG87-80 SEG0-68 SEG69-79	A A Ianual	Table Initial status ⁺¹ Hi-Z / O (L)+2 Hi-Z / O (L)+2 Hi-Z / O (L)+2 Hi-Z / O (L)+2	- * 17.2.1.1 Lis Common d General pu Segment d General pu	LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin Indicates the status when the pin is configured for LCD8A st of LCD16A Pins Function lata output pins rpose IO/common data output/segment data output pins ata output pins rpose IO/segment data output pins
CP1 CP2 1C17M10 Technical M Fror) Pin name COM0-7 COM8-15/SEG87-80 SEG0-68 SEG0-68 SEG69-79 LFRO	A A lanual	Table Initial status ⁺¹ Hi-Z / O (L)+2 Hi-Z / O (L)+2 Hi-Z / O (L)+2	- * 17.2.1.1 Lis Common d General pu Segment d General pu Frame sign	LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin Indicates the status when the pin is configured for LCD8A st of LCD16A Pins Function lata output pins rpose IO/common data output/segment data output pins ata output pins rpose IO/segment data output pins ala monitoring output pin
CP1 CP2 1C17M10 Technical M Error) Pin name COM0-7 COM8-15/SEG87-80 SEG0-68 SEG0-68 SEG69-79 LFRO VC1-5	A A lanual 0 0 0 0 0 0 0	Table Initial status ⁺¹ Hi-Z / O (L)+2 Hi-Z / O (L)+2 Hi-Z / O (L)+2 Hi-Z / O (L)+2	- * 17.2.1.1 Lis Common d General pu Segment d General pu Frame sign LCD panel	LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin Indicates the status when the pin is configured for LCD8A st of LCD16A Pins Function lata output pins rpose IO/common data output/segment data output pins ata output pins rpose IO/segment data output pins ata output pins rpose IO/segment data output pins ala monitoring output pin drive power supply pins
CP1 CP2 1C17M10 Technical M Error) Pin name COM0-7 COM8-15/SEG87-80 SEG0-68 SEG0-68 SEG69-79 LFRO VC1-5 CP1-5 CP1-5	A A Ianual	Table Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) -	- * Common d General pu Segment d General pu Frame sign LCD panel LCD voltag	LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin Indicates the status when the pin is configured for LCD8A st of LCD16A Pins Function lata output pins rpose IO/common data output/segment data output pins ata output pins rpose IO/segment data output pins ala monitoring output pin
CP1 CP2 1C17M10 Technical M Error) Pin name COM0-7 COM8-15/SEG87-80 SEG0-68 SEG69-79 LFRO VC1-5 CP1-5 *1: Indica Correct)	A A Ianual	Table Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) - - status when the Table	- * 17.2.1.1 Lis Common d General pu Frame sign LCD panel LCD voltag pin is confi	LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin Indicates the status when the pin is configured for LCD8A st of LCD16A Pins Function lata output pins rpose IO/common data output/segment data output pins ata output pins rpose IO/segment data output pins all monitoring output pin drive power supply pins je booster capacitor connecting pins gured for LCD16A. *2: When LCD16CTL.LCDDIS bit = 1 st of LCD16A Pins
CP1 CP2 1C17M10 Technical M Error) Pin name COM0-7 COM8-15/SEG87-80 SEG0-68 SEG0-68 SEG0-68 SEG0-68 SEG0-68 SEG0-79 LFRO Vc1-5 CP1-5 *1: Indica Correct) Pin name	A A Ianual	Table Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) - status when the Table Initial status*1	- * 17.2.1.1 Lis Common d General pu Segment d General pu Frame sign LCD panel LCD voltag pin is confi 17.2.1.1 Lis	LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin Indicates the status when the pin is configured for LCD8A st of LCD16A Pins Function lata output pins rpose IO/common data output/segment data output pins rpose IO/segment data output pins ial monitoring output pin drive power supply pins je booster capacitor connecting pins gured for LCD16A. *2: When LCD16CTL.LCDDIS bit = 1 st of LCD16A Pins Function
CP1 CP2 1C17M10 Technical M Fror) Pin name COM0-7 COM8-15/SEG87-80 SEG0-68 SEG69-79 LFRO VC1-5 CP1-5 *1: Indica Correct) Pin name COM0-7	A A A Ianual	Table Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) status when the Table Initial status*1 Hi-Z / O (L)*2	- * 17.2.1.1 Lis Common d General pu Segment d General pu Frame sign LCD panel LCD voltag pin is confi 17.2.1.1 Lis Common d	LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin Indicates the status when the pin is configured for LCD8A st of LCD16A Pins Function lata output pins rpose IO/common data output/segment data output pins rpose IO/segment data output pins ial monitoring output pin drive power supply pins je booster capacitor connecting pins gured for LCD16A. *2: When LCD16CTL.LCDDIS bit = 1 st of LCD16A Pins Function
CP1 CP2 1C17M10 Technical M Error) Pin name COM0-7 COM8-15/SEG87-80 SEG0-68 SEG69-79 LFRO Vc1-5 CP1-5 *1: Indica Correct) Pin name COM0-7 COM0-7	A A A Ianual	Table Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) - status when the Table Initial status*1 Hi-Z / O (L)*2	- * 17.2.1.1 Lis Common d General pu Segment d General pu LCD voltag pin is confi 17.2.1.1 Lis Common d General pu	LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin Indicates the status when the pin is configured for LCD8A st of LCD16A Pins Function lata output pins rpose IO/common data output/segment data output pins rpose IO/segment data output pins je booster capacitor connecting pins gured for LCD16A. *2: When LCD16CTL.LCDDIS bit = * st of LCD16A Pins Function
CP1 CP2 CP2 IC17M10 Technical M Tror) Pin name COM0-7 COM8-15/SEG87-80 SEG0-68 SEG69-79 LFRO Vc1-5 CP1-5 *1: Indica Correct) Pin name COM0-7 COM8-15/SEG87-80 SEG0-68 SEG0-68	A A A Ianual	Table Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) - status when the Initial status*1 Hi-Z / O (L)*2	- * 17.2.1.1 Lis Common d General pu Segment d General pu LCD panel LCD voltag pin is confi 17.2.1.1 Lis Common d General pu Segment d	LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin Indicates the status when the pin is configured for LCD8A st of LCD16A Pins Function lata output pins rpose IO/common data output/segment data output pins rpose IO/segment data output pins ual monitoring output pin drive power supply pins ge booster capacitor connecting pins gured for LCD16A. *2: When LCD16CTL.LCDDIS bit = 1 st of LCD16A Pins Function
CP1 CP2 CP2 IC17M10 Technical M Tror) Pin name COM0-7 COM8-15/SEG87-80 SEG60-68 SEG69-79 LFRO Vc1-5 CP1-5 *1: Indica Correct) Pin name COM0-7 COM8-15/SEG87-80 SEG0-68 SEG0-68 SEG0-79 *1: Indica	A A A Ianual $I/0^{-1}$ O O O O O P A ates the II/O_1^1 A A A A A A	Table Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) - - status when the Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2	- * 17.2.1.1 Lis Common d General pu Segment d General pu LCD panel LCD voltag pin is confi 17.2.1.1 Lis Common d General pu Segment d General pu	LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin Indicates the status when the pin is configured for LCD8A st of LCD16A Pins Function lata output pins rpose IO/common data output/segment data output pins ial monitoring output pin drive power supply pins je booster capacitor connecting pins gured for LCD16A. *2: When LCD16CTL.LCDDIS bit = * st of LCD16A Pins Function
CP1 CP2 CP2 IC17M10 Technical M irror) Pin name COM0-7 COM8-15/SEG87-80 SEG0-68 SEG0-68 SEG0-68 SEG0-68 Vc1-5 CP1-5 Vc1-5 *1: Indica Correct) Pin name COM0-7 COM8-15/SEG87-80 SEG0-68 SEG0-68 SEG0-68 SEG0-79 LFRO Yen name COM0-7 COM8-15/SEG87-80 SEG0-68 SEG0-68 SEG0-68 SEG69-79 LFRO Yen name	$ I/O^{-1} $ A Ianual Ianual I/O^{-1} O O O O O O A ates the II/O^{1} A' A' A' A' A' A' O	Table Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) - status when the Initial status*1 Hi-Z / O (L)*2	- * 17.2.1.1 Lis Common d General pu Segment d General pu LCD panel LCD voltag pin is confi 17.2.1.1 Lis Common d General pu Segment d General pu Segment d	LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin Indicates the status when the pin is configured for LCD8A st of LCD16A Pins Function lata output pins rpose IO/common data output/segment data output pins rpose IO/segment data output pins gured for LCD16A. *2: When LCD16CTL.LCDDIS bit = st of LCD16A Pins Function
CP1 CP2 CP2 IC17M10 Technical M Tror) Pin name COM0-7 COM8-15/SEG87-80 SEG60-68 SEG69-79 LFRO Vc1-5 CP1-5 *1: Indica Correct) Pin name COM0-7 COM8-15/SEG87-80 SEG0-68 SEG0-68 SEG0-79 *1: Indica	A A A Ianual $I/0^{-1}$ O O O O O P A ates the II/O_1^1 A A A A A A	Table Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) - - status when the Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2	- * 17.2.1.1 Lis Common d General pu Segment d General pu LCD panel LCD voltag pin is confi 17.2.1.1 Lis Common d General pu Segment d General pu Segment d General pu	LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin Indicates the status when the pin is configured for LCD8A st of LCD16A Pins Function lata output pins rpose IO/common data output/segment data output pins ial monitoring output pin drive power supply pins je booster capacitor connecting pins gured for LCD16A. *2: When LCD16CTL.LCDDIS bit = st of LCD16A Pins Function

ror)				
			Т	able 18.2.1.1 List of LCD8A Pins
Pin name		I/O*1	Initial status ⁺¹	Function
COM0-3		Α	Hi-Z / O (Vss)*2	Common data output pins
COM4-7/SEG	0–3	Α	Hi-Z / O (Vss)*2	Common data output/segment data output pins
SEG4-49		Α	Hi-Z / O (Vss)*2	Segment data output pins (See Table 18.2.1.2.)
LFRO		0	O (L)	Frame signal monitoring output pin
Vci		Р	-	LCD panel drive power supply pin
VC2		Р	-	LCD panel drive power supply pin
Vсз		Р	-	LCD panel drive power supply pin
CP1		Α	-	LCD voltage booster capacitor connecting pin (S1C17M31/M33/M34)
CP2		Α	-	LCD voltage booster capacitor connecting pin (S1C17M31/M33/M34)
prrect)				
				able 18.2.1.1 List of LCD8A Pins
Pin name COM0-3		_I/O <u>1</u>	Initial status*1	Function
COMU-3 COM4-7/SEG	0.0	A		Common data output pins Common data output/segment data output pins
SEG4-49	10-3	A	. ,	Segment data output pins (See Table 18.2.1.2.)
LFRO		<u>A</u> (0		
	-+	P	O (L)	Frame signal monitoring output pin
VC1 VC2	\rightarrow	<u>-</u> Р	-	LCD panel drive power supply pin LCD panel drive power supply pin
VC2 VC3	-+	P	_	LCD panel drive power supply pin
VC3 CP1		A	_	LCD voltage booster capacitor connecting pin (S1C17M31/M33/M34)
CP1 CP2	-+	A		LCD voltage booster capacitor connecting pin (S1C17M31/M33/M34)
	*1:	Indicate		1 5
C17W13 Tec ror)				
ror)	shnica	ıl Manu	ıal	Table 18.2.1.1 List of LCD4A Pins
ror)	chnica	Il Manu	ıal - tatus∗1	
ror) Pin name I	hnica	Initial st Hi-Z / (ıal tatus⁺1 O (L)⁺2 Commor	Table 18.2.1.1 List of LCD4A Pins Function
ror) Pin name I COM0-3	2hnica	Initial st Hi-Z / (Hi-Z / (tatus*1 O (L)*2 Commor O (L)*2 Segment	Table 18.2.1.1 List of LCD4A Pins Function n data output-only pins
Pin name I COM0-3 SEG0-1 SEG2-7 SEG8-19	bhnica	Initial st Hi-Z / (Hi-Z / (Hi-Z / (Hi-Z / (tatus*1 O (L)*2 O (L)*2 Commor O (L)*2 Segment O (L)*2 Segment O (L)*2 Segment O (L)*2	Table 18.2.1.1 List of LCD4A Pins Function n data output-only pins t data output-only pins (Not available in the SQFN7-48pin package) t data output-only pins purpose IO/segment data output pins
Pin name I COM0-3 SEG0-1 SEG2-7 SEG8-19 SEG20-21 SEG20-21	2/0+1 0 0 0 0	Initial st Hi-Z / (Hi-Z / (Hi-Z / (Hi-Z / (Hi-Z / (tatus*1 O (L)*2 O (L)*2 Commor O (L)*2 Segment O (L)*2 Segment O (L)*2 Segment O (L)*2 Segment	Table 18.2.1.1 List of LCD4A Pins Function n data output-only pins t data output-only pins (Not available in the SQFN7-48pin package) t data output-only pins purpose IO/segment data output pins t data output-only pins (Not available in the 48-pin package)
Pin name I COM0-3 SEG0-1 SEG2-7 SEG8-19 SEG20-21 SEG20-21	2hnica 0 0 0 0 0	Initial st Hi-Z / (Hi-Z / (Hi-Z / (Hi-Z / (Hi-Z / (Hi-Z / (tatus*1 O (L)*2 O (L)*2 Commor O (L)*2 Segment O (L)*2 S	Table 18.2.1.1 List of LCD4A Pins Function data output-only pins t data output-only pins t data output-only pins purpose IO/segment data output pins t data output-only pins (Not available in the 48-pin package) purpose IO/segment data output pins t data output-only pins (Not available in the 48-pin package) purpose IO/segment data output pins (Not available in the 48-pin package)
Pin name I COM0-3 SEG0-1 SEG2-7 SEG8-19 SEG20-21 SEG20-21 SEG22-25 LFRO	2hnica	Initial st Hi-Z / (Hi-Z / (Hi-Z / (Hi-Z / (Hi-Z / (tatus*1 O (L)*2 O (L)*2 Commor O (L)*2 Segment O (L)*2 Segment D (L)*2 S	Table 18.2.1.1 List of LCD4A Pins Function n data output-only pins t data output-only pins t data output-only pins purpose IO/segment data output pins t data output-only pins (Not available in the 48-pin package) t data output-only pins purpose IO/segment data output pins t data output-only pins (Not available in the 48-pin package) purpose IO/segment data output pins (Not available in the TQFP12-48pin package) gnal monitoring output pin (Not available in the TQFP12-48pin package)
Pin name I COM0-3 SEG0-1 SEG2-7 SEG8-19 SEG20-21 SEG20-21 SEG22-25 LFRO Vc1 Vc1	2hnica 0 0 0 0 0 0 0	Initial st Hi-Z / (Hi-Z / (Hi-Z / (Hi-Z / (Hi-Z / (Hi-Z / (O ()	tatus*1 O (L)*2 Commor O (L)*2 Segment O (L)*2 Segment O (L)*2 Segment O (L)*2 Segment O (L)*2 General- D (L)*2 CO (L)*2 CO (L)*2 CO (L)*2 CO (L)*2 CO (L)*2 CO (L)*2	Table 18.2.1.1 List of LCD4A Pins Function n data output-only pins t data output-only pins (Not available in the SQFN7-48pin package) t data output-only pins purpose IO/segment data output pins t data output-only pins (Not available in the 48-pin package) t data output-only pins purpose IO/segment data output pins t data output-only pins (Not available in the 48-pin package) purpose IO/segment data output pins (Not available in the 48-pin package) purpose IO/segment data output pins (Not available in the TQFP12-48pin package) gnal monitoring output pin (Not available in the TQFP12-48pin package) el drive power supply pin
Pin name I COM0-3 SEG0-1 SEG2-7 SEG8-19 SEG20-21 SEG20-21 SEG22-25 LFRO Vc1 Vc2	2hnica 0 0 0 0 0 0 P P	Initial st Hi-Z / (Hi-Z / (Hi-Z / (Hi-Z / (Hi-Z / (O (tatus*1 O (L)*2 Commor O (L)*2 Segment O (L)*2 Segment CD Pan Segment Segme	Table 18.2.1.1 List of LCD4A Pins Function In data output-only pins t data output-only pins (Not available in the SQFN7-48pin package) t data output-only pins purpose IO/segment data output pins t data output-only pins (Not available in the 48-pin package) purpose IO/segment data output pins (Not available in the 48-pin package) purpose IO/segment data output pins (Not available in the TQFP12-48pin package) gnal monitoring output pin (Not available in the TQFP12-48pin package) iel drive power supply pin iel drive power supply pin
Pin name I COM0-3 SEG0-1 SEG2-7 SEG8-19 SEG20-21 SEG20-21 SEG22-25 LFRO Vc1 Vc2 Vc3 Vc3	2hnica 0 0 0 0 0 0 0 P P P	Initial st Hi-Z/(Hi-Z/(Hi-Z/(Hi-Z/(Hi-Z/(O(- - -	tatus*1 O (L)*2 Commor O (L)*2 Segment O (L)*2 Segment CD pan CD pan CD pan CD pan	Table 18.2.1.1 List of LCD4A Pins Function In data output-only pins t data output-only pins (Not available in the SQFN7-48pin package) t data output-only pins purpose IO/segment data output pins t data output-only pins (Not available in the 48-pin package) purpose IO/segment data output pins (Not available in the 48-pin package) purpose IO/segment data output pins (Not available in the TQFP12-48pin package) pel drive power supply pin el drive power supply pin el drive power supply pin
Pin name I COM0-3 SEG0-1 SEG2-7 SEG8-19 SEG20-21 SEG20-21 SEG22-25 LFRO Vc1 Vc2	2hnica 0 0 0 0 0 0 P P	Initial st Hi-Z / (Hi-Z / (Hi-Z / (Hi-Z / (Hi-Z / (O (tatus*1 O (L)*2 Commor O (L)*2 Segment O (L)*2 Segment CD pan Segment Segme	Table 18.2.1.1 List of LCD4A Pins Function n data output-only pins t data output-only pins t data output-only pins purpose IO/segment data output pins t data output-only pins (Not available in the 48-pin package) purpose IO/segment data output pins t data output-only pins (Not available in the 48-pin package) purpose IO/segment data output pins (Not available in the 48-pin package) purpose IO/segment data output pins (Not available in the TQFP12-48pin package) purpose Idrive power supply pin el drive power supply pin el drive power supply pin age booster capacitor connecting pin
Pin name I COM0-3 SEG0-1 SEG2-7 SEG8-19 SEG20-21 SEG22-25 LFRO Vc1 Vc2 Vc3 CP1 CP1	2hnica 0 0 0 0 0 P P P A	Initial st Hi-Z/(Hi-Z/(Hi-Z/(Hi-Z/(Hi-Z/(O(- - -	tatus*1 D (L)*2 Commor D (L)*2 Segment D (L)*2 Segment D (L)*2 Segment D (L)*2 General- D (L)*2 General- CD pan CD pan (Not avai	Table 18.2.1.1 List of LCD4A Pins Function n data output-only pins t data output-only pins (Not available in the SQFN7-48pin package) t data output-only pins purpose IO/segment data output pins t data output-only pins (Not available in the 48-pin package) purpose IO/segment data output pins (Not available in the 48-pin package) purpose IO/segment data output pins (Not available in the 48-pin package) purpose IO/segment data output pins (Not available in the TQFP12-48pin package) el drive power supply pin el drive power supply pin el drive power supply pin age booster capacitor connecting pin lable in the TQFP12-48pin package)
Pin name I COM0-3 SEG0-1 SEG2-7 SEG8-19 SEG20-21 SEG20-21 SEG22-25 LFRO Vc1 Vc2 Vc3 Vc3	2hnica 0 0 0 0 0 0 0 P P P	Initial st Hi-Z/(Hi-Z/(Hi-Z/(Hi-Z/(Hi-Z/(O(- - -	tatus*1 D (L)*2 Commor D (L)*2 Commor D (L)*2 Segment D (L)*2 Segment D (L)*2 General- D (L)*2 General- LCD pan CD pan CD pan CD pan LCD pan CD pan	Table 18.2.1.1 List of LCD4A Pins Function n data output-only pins t data output-only pins t data output-only pins purpose IO/segment data output pins t data output-only pins (Not available in the 48-pin package) purpose IO/segment data output pins t data output-only pins (Not available in the 48-pin package) purpose IO/segment data output pins (Not available in the 48-pin package) purpose IO/segment data output pins (Not available in the TQFP12-48pin package) purpose Idrive power supply pin el drive power supply pin el drive power supply pin age booster capacitor connecting pin

(Correct)				Table 18.2.1.1 List of LCD4A Pins
Pin name		Initial s	tatus*1	Function
COM0-3	A			on data output-only pins
SEG0-1	Α			nt data output-only pins (Not available in the SQFN7-48pin package)
SEG2-7	A			nt data output only pins
SEG8-19	A		., .	al-purpose IO/segment data output pins
SEG20-21	A			nt data output-only pins (Not available in the 48-pin package)
SEG20-21				al-purpose IO/segment data output pins (Not available in the 48-pin package)
	A			
LFRO	0	0(signal monitoring output pin (Not available in the TQFP12-48pin package)
Vc1	P	-		anel drive power supply pin
Vc2	Р			anel drive power supply pin
Vc3	Р	-		anel drive power supply pin
CP1	Α	-		oltage booster capacitor connecting pin railable in the TQFP12-48pin package)
CP2	Α	-	LCD vo	oltage booster capacitor connecting pin
			(Not av	ailable in the TQFP12-48pin package)
	*1	: Indica	tes the status	when the pin is configured for LCD4A. *2: When LCD4CTL.LCDDIS bit = 1
S1C17W14/W	16 Te	chnical	Manual	
(Error)				
				Table 18.2.1.1 List of LCD8B Pins
Pin name	9	I/O+1	Initial status*1	Function
COM0-3		0	Hi-Z / O (L)*2	Common data output-only pin
COM4-7/SEC	30-3	0		Common data output/segment data output pin
		0		Segment data output-only pin
SEG4-41(W1 SEG4-46(W1	· ·	0	HI-Z / U (L)*2	Segment data output-only pin
SEG42-53(W SEG47-59(W		0	Hi-Z / O (L)*2	General-purpose IO/segment data output pin
LFRO		0	O (L)	Frame signal monitoring output pin
Vc1		Р	_	LCD panel drive power supply pin
Vc2		P	_	LCD panel drive power supply pin
Vc3		P		LCD panel drive power supply pin
		· ·	_	
CP1		A	-	LCD voltage booster capacitor connecting pin
CP2		Α	-	LCD voltage booster capacitor connecting pin
(Correct)	*1:	Indicate	es the status w	when the pin is configured for LCD8B. *2: When LCD8CTL.LCDDIS bit = 1
				Table 18.2.1.1 List of LCD8B Pins
Pin name	•	_"	Initial status*1	Function
COM0-3		A		Common data output-only pin
COM4-7/SEC		A		Common data output/segment data output pin
SEG4-41(W1 SEG4-46(W1		A	Hi-Z / O (L)*2	Segment data output-only pin
SEG42-53(W SEG47-59(W	/14)	A	Hi-Z / O (L)*2	General-purpose IO/segment data output pin
LFRO	,	0	0(1)	Frame signal monitoring output pin
			0 (L)	
Vc1		P	_	LCD panel drive power supply pin
Vc2		P	-	LCD panel drive power supply pin
Vсз		Р	-	LCD panel drive power supply pin
CP1		Α	-	LCD voltage booster capacitor connecting pin
CP2		Α	-	LCD voltage booster capacitor connecting pin
	*1:	Indicate	es the status w	when the pin is configured for LCD8B. *2: When LCD8CTL.LCDDIS bit = 1

rror)			
			Table 17.2.1.1 List of LCD8B Pins
Pin name	I/O*1	Initial status*1	Function
COM0-3	0		Common data output-only pin
COM4-7/SEG0-3	0		Common data output/segment data output pin
SEG4-15	0	Hi-Z / O (L)*2	Segment data output-only pin
SEG16-23	0	O (L)	General-purpose IO/segment data output pin
SEG24-27	0		Segment data output-only pin (Not available in the 64-pin package)
SEG28-29	0		Segment data output-only pin (Not available in the 64-pin/80-pin package)
SEG30-33	0	Hi-Z / O (L)*2	Segment data output-only pin (Not available in the 64-pin package)
Vc1	P	-	LCD panel drive power supply pin
Vc2	P	-	LCD panel drive power supply pin
Vc3	P	-	LCD panel drive power supply pin
Vc4	P	-	LCD panel drive power supply pin
CP1	A	-	LCD voltage booster capacitor connecting pin
CP2 CP3	A	_	LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin
CP3 CP4	A		LCD voltage booster capacitor connecting pin
*1.	indicat	es the status w	hen the pin is configured for LCD8B. *2: When LCD8CTL.MODEN bit = 1
orrect)			
			Table 17.2.1.1 List of LCD8B Pins
Pin name	[/O ¹ A)	Initial status*1	Function
Pin name COM0-3	A)	Initial status*1 Hi-Z / O (L)*2	Function Common data output-only pin
Pin name COM0-3 COM4-7/SEG0-3		Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2	Function
Pin name COM0-3 COM4-7/SEG0-3 SEG4-15	A) A)	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2	Function Common data output-only pin Common data output/segment data output pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-15 SEG16-23	A) A) A)	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L)	Function Common data output-only pin Common data output/segment data output pin Segment data output-only pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-15 SEG16-23 SEG24-27	A) A) A) A)	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) Hi-Z / O (L)*2	Function Common data output-only pin Common data output/segment data output pin Segment data output-only pin General-purpose IO/segment data output pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-15 SEG16-23 SEG24-27 SEG28-29	A) A) A) A) A) A)	$\begin{array}{c} \mbox{Initial status}^{*1} \\ \mbox{Hi-Z} \ / \ O \ (L)^{*2} \\ \mbox{Hi-Z} \ / \ O \ (L)^{*2} \\ \mbox{Hi-Z} \ / \ O \ (L)^{*2} \\ \mbox{O} \ (L) \\ \mbox{Hi-Z} \ / \ O \ (L)^{*2} \\ \mbox{Hi-Z} \ / \ O \ (L)^{*2} \end{array}$	Function Common data output-only pin Common data output/segment data output pin Segment data output-only pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package)
Pin name COM0-3 COM4-7/SEG0-3 SEG4-15 SEG16-23 SEG24-27 SEG28-29 SEG30-33	A) A) A) A) A) A) A)	$\begin{array}{c} \mbox{Initial status}^{*1} \\ \mbox{Hi-Z} / O (L)^{*2} \\ \mbox{Hi-Z} / O (L)^{*2} \\ \mbox{Hi-Z} / O (L)^{*2} \\ \mbox{O} (L) \\ \mbox{Hi-Z} / O (L)^{*2} \end{array}$	Function Common data output-only pin Common data output/segment data output pin Segment data output-only pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin package) LCD panel drive power supply pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-15 SEG16-23 SEG24-27 SEG28-29 SEG30-33 Vc1 Vc2	A) A) A) A) A) A) A) A) P P	$\begin{array}{c} \mbox{Initial status}^{*1} \\ \mbox{Hi-Z} / O (L)^{*2} \\ \mbox{Hi-Z} / O (L)^{*2} \\ \mbox{Hi-Z} / O (L)^{*2} \\ \mbox{O} (L) \\ \mbox{Hi-Z} / O (L)^{*2} \end{array}$	Function Common data output-only pin Common data output/segment data output pin Segment data output-only pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin package) LCD panel drive power supply pin LCD panel drive power supply pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-15 SEG16-23 SEG24-27 SEG28-29 SEG30-33 Vc1 Vc2 Vc3	A) A) A) A) A) A) A) A) P P P	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 - - -	Function Common data output-only pin Common data output/segment data output pin Segment data output-only pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) LCD panel drive power supply pin LCD panel drive power supply pin LCD panel drive power supply pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-15 SEG16-23 SEG24-27 SEG28-29 SEG30-33 Vc1 Vc2 Vc3 Vc4	A) A) A) A) A) A) A) P P P P	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) Hi-Z / O (L)*2 - - - - -	Function Common data output-only pin Common data output/segment data output pin Segment data output-only pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) LCD panel drive power supply pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-15 SEG16-23 SEG24-27 SEG28-29 SEG30-33 Vc1 Vc2 Vc3 Vc4 CP1	A) A) A) A) A) A) A) P P P A	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) Hi-Z / O (L)*2 - - - - - - - - - - - - -	Function Common data output-only pin Common data output/segment data output pin Segment data output-only pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin package) LCD panel drive power supply pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-15 SEG16-23 SEG24-27 SEG28-29 SEG30-33 Vc1 Vc2 Vc3 Vc4 CP1 CP2	A) A) A) A) A) A) P P P P P A A	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 	Function Common data output-only pin Common data output/segment data output pin Segment data output-only pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin package) LCD panel drive power supply pin LCD voltage booster capacitor connecting pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-15 SEG16-23 SEG24-27 SEG30-33 Vc1 Vc2 Vc3 Vc4 CP1 CP2 CP3	A) A) A) A) A) A) P P P P P A A A A	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) Hi-Z / O (L)*2 - - - - - - - - - - - - -	Function Common data output-only pin Common data output/segment data output pin Segment data output-only pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin package) LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-15 SEG16-23 SEG24-27 SEG30-33 Vc1 Vc2 Vc3 Vc4 CP1 CP2 CP3 CP4	A) A) A) A) A) A) A) A) A) P P P P P A A A A A	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 	Function Common data output-only pin Common data output/segment data output pin Segment data output-only pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin package) LCD panel drive power supply pin LCD voltage booster capacitor connecting pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-15 SEG16-23 SEG24-27 SEG30-33 Vc1 Vc2 Vc3 Vc4 CP1 CP2 CP3 CP4	A) A) A) A) A) A) A) A) A) P P P P P A A A A A	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 	Function Common data output-only pin Common data output/segment data output pin Segment data output-only pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin package) LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-15 SEG16-23 SEG24-27 SEG30-33 Vc1 Vc2 Vc3 Vc4 CP1 CP2 CP3 CP4	A) A) A) A) A) A) A) A) A) P P P P P A A A A A	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 	Function Common data output-only pin Common data output/segment data output pin Segment data output-only pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin package) LCD panel drive power supply pin LCD voltage booster capacitor connecting pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-15 SEG16-23 SEG24-27 SEG30-33 Vc1 Vc2 Vc3 Vc4 CP1 CP2 CP3 CP4	A) A) A) A) A) A) A) A) A) P P P P P A A A A A	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 	Function Common data output-only pin Common data output/segment data output pin Segment data output-only pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin package) LCD panel drive power supply pin LCD voltage booster capacitor connecting pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-15 SEG16-23 SEG24-27 SEG30-33 Vc1 Vc2 Vc3 Vc4 CP1 CP2 CP3 CP4	A) A) A) A) A) A) A) A) A) P P P P P A A A A A	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 	Function Common data output-only pin Common data output/segment data output pin Segment data output-only pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin package) LCD panel drive power supply pin LCD voltage booster capacitor connecting pin
COM0-3 COM4-7/SEG0-3 SEG4-15 SEG16-23 SEG24-27 SEG28-29 SEG30-33 Vc1 Vc2 Vc2 Vc3 Vc4 CP1 CP2 CP3 CP4	A) A) A) A) A) A) A) A) A) P P P P P A A A A A	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 	Function Common data output-only pin Common data output/segment data output pin Segment data output-only pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin package) LCD panel drive power supply pin LCD voltage booster capacitor connecting pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-15 SEG16-23 SEG24-27 SEG30-33 Vc1 Vc2 Vc3 Vc4 CP1 CP2 CP3 CP4	A) A) A) A) A) A) A) A) A) P P P P P A A A A A	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 	Function Common data output-only pin Common data output/segment data output pin Segment data output-only pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin package) LCD panel drive power supply pin LCD voltage booster capacitor connecting pin

			Table 18.2.1.1 List of LCD8B Pins
Pin name	I/O*1	Initial status*1	Function
COM0-3	0		General-purpose IO/Common data output-only pin
COM4-7/SEG0-3	Ö		General-purpose IO/Common data output/segment data output pin
SEG4-23	ŏ		General-purpose IO/segment data output pin
SEG24-27	0		Segment data output-only pin (Not available in the 64-pin package)
SEG28-34	0		Segment data output-only pin (Not available in the 64-pin/80-pin package)
SEG35-38	0		Segment data output-only pin (Not available in the 64-pin package)
SEG39-47	0		Segment data output-only pin (Not available in the 64-pin/80-pin package)
LFRO	0	O (L)	Frame signal monitoring output pin
Vc1	Р	-	LCD panel drive power supply pin
VC2	Р	_	LCD panel drive power supply pin
Vсз	Р	-	LCD panel drive power supply pin
VC4	Р	-	LCD panel drive power supply pin
Срі	Α	_	LCD voltage booster capacitor connecting pin
CP2	Α	-	LCD voltage booster capacitor connecting pin
Срз	Α	-	LCD voltage booster capacitor connecting pin
Cp4	Α	-	LCD voltage booster capacitor connecting pin
*1.	Indicat	es the status w	hen the pin is configured for LCD8B. *2: When LCD8CTL.LCDDIS bit = 1
orrect)			
orrect)			Table 18.2.1.1 List of LCD8B Pins
orrect) Pin name		Initial status*1	Table 18.2.1.1 List of LCD8B Pins
Pin name		Initial status*1	
Pin name COM0–3		Initial status*1 Hi-Z / O (L)*2	Function
Pin name COM0-3 COM4-7/SEG0-3	A	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2	Function General-purpose IO/Common data output-only pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-23	A	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2	Function General-purpose IO/Common data output-only pin General-purpose IO/Common data output/segment data output pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-23 SEG24-27	A A A A A	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2 Hi-Z / O (L)*2	Function General-purpose IO/Common data output-only pin General-purpose IO/Common data output/segment data output pin General-purpose IO/segment data output pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-23 SEG24-27 SEG28-34	A A A A A A A	$\begin{array}{c} \mbox{Initial status}^{*1} \\ \mbox{Hi-Z} \ / \ O \ (L)^{*2} \end{array}$	Function General-purpose IO/Common data output-only pin General-purpose IO/Common data output/segment data output pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin package)
Pin name COM0-3 COM4-7/SEG0-3 SEG4-23 SEG24-27 SEG28-34 SEG35-38	A A A A A	$\begin{array}{c} \mbox{Initial status}^{*1} \\ \mbox{Hi-Z} \ / \ O \ (L)^{*2} \end{array}$	Function General-purpose IO/Common data output-only pin General-purpose IO/Common data output/segment data output pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package)
Pin name COM0-3 COM4-7/SEG0-3 SEG4-23 SEG24-27 SEG28-34 SEG35-38 SEG39-47 LFRO	A A A A A A A A O	$\begin{array}{c} \mbox{Initial status}^{*1} \\ \mbox{Hi-Z} \ / \ O \ (L)^{*2} \end{array}$	Function General-purpose IO/Common data output-only pin General-purpose IO/Common data output/segment data output pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Frame signal monitoring output pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-23 SEG24-27 SEG28-34 SEG35-38 SEG39-47 LFRO Vc1	A A Ai Ai Ai Ai Ai Ai O P	Initial status*1 Hi-Z / O (L)*2 O (L) -	Function General-purpose IO/Common data output-only pin General-purpose IO/Common data output/segment data output pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Frame signal monitoring output pin LCD panel drive power supply pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-23 SEG24-27 SEG28-34 SEG35-38 SEG39-47 LFRO Vc1 Vc2	A A A A A A A A A A A C A C C P P	Initial status*1 Hi-Z / O (L)*2 O (L) - -	Function General-purpose IO/Common data output-only pin General-purpose IO/Common data output/segment data output pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Frame signal monitoring output pin LCD panel drive power supply pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-23 SEG24-27 SEG28-34 SEG35-38 SEG39-47 LFRO Vc1 Vc2 Vc3	A A A A A A A A O P P P P	Initial status*1 Hi-Z / O (L)*2 O (L) -	Function General-purpose IO/Common data output-only pin General-purpose IO/Common data output/segment data output pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Frame signal monitoring output pin LCD panel drive power supply pin LCD panel drive power supply pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-23 SEG24-27 SEG28-34 SEG35-38 SEG39-47 LFRO Vc1 Vc2 Vc3	A A A A A A A A A O P P P P P	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) - - - -	Function General-purpose IO/Common data output-only pin General-purpose IO/Common data output/segment data output pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Frame signal monitoring output pin LCD panel drive power supply pin LCD panel drive power supply pin LCD panel drive power supply pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-23 SEG24-27 SEG35-38 SEG39-47 LFRO Vc1 Vc2 Vc3 Vc4 CP1	A A Ai Ai Ai Ai Ai Ai O P P P P P A	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) - - - - - -	Function General-purpose IO/Common data output-only pin General-purpose IO/Common data output/segment data output pin General-purpose IO/segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Frame signal monitoring output pin LCD panel drive power supply pin
Pin name COM0–3 COM4–7/SEG0–3 SEG4–23 SEG24–27 SEG35–38 SEG39–47 LFRO Vc1 Vc2 Vc3 Vc4 CP1 CP2	A A Ai Ai Ai Ai Ai Ai P P P P P A A	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) - - - -	Function General-purpose IO/Common data output-only pin General-purpose IO/Common data output/segment data output pin General-purpose IO/Segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Frame signal monitoring output pin LCD panel drive power supply pin LCD panel drive power supply pin LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin
Pin name COM0-3 COM4-7/SEG0-3 SEG4-23 SEG24-27 SEG28-34 SEG35-38 SEG39-47 LFRO Vc1 Vc2 Vc3 Vc4 CP1 CP2 CP3	A A A A A A A O P P P P A A A	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) - - - - - - - - -	Function General-purpose IO/Common data output-only pin General-purpose IO/Common data output/segment data output pin General-purpose IO/Segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Frame signal monitoring output pin LCD panel drive power supply pin LCD panel drive power supply pin LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin
COM0-3 COM4-7/SEG0-3 SEG4-23 SEG24-27 SEG28-34 SEG35-38 SEG39-47 LFRO Vc1 Vc2 Vc3 Vc4 CP1 CP2 CP3 CP4	A A A A A A A A O P P P P P A A A A A	Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2 O (L) - - - - - - - - - - - - -	Function General-purpose IO/Common data output-only pin General-purpose IO/Common data output/segment data output pin General-purpose IO/Segment data output pin Segment data output-only pin (Not available in the 64-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Segment data output-only pin (Not available in the 64-pin/80-pin package) Frame signal monitoring output pin LCD panel drive power supply pin LCD panel drive power supply pin LCD panel drive power supply pin LCD voltage booster capacitor connecting pin LCD voltage booster capacitor connecting pin

rror)					
		Table 1	8.2.1.1 Lis	st of LCD24A Pins	
Pin name	I/O*1	Initia	I status*1	Function	
SEG53-0	0		/ O (L)+2	Segment data output-only pin	
COM7-0	0		/ O (L)*2	Common data output-only pin	
SEG71-54	0		0 (L)	General-purpose IO/segment data output pin	
COM23-8	0		0 (L)	General-purpose IO/common data output pin	
LFRO	0		0 (L)	Frame signal monitoring output pin	
Vc1	P		_	LCD panel drive power supply pin	
Vc2	P		_	LCD panel drive power supply pin	
Vc3	P		_	LCD panel drive power supply pin	
Vc4	P		_	LCD panel drive power supply pin	
CP1	A		_	LCD voltage booster capacitor connecting pin	
CP2	A		_	LCD voltage booster capacitor connecting pin	
Срз	A		_	LCD voltage booster capacitor connecting pin	
CP4	A		_	LCD voltage booster capacitor connecting pin	
				gured for LCD24A. *2: When LCD24CTL.MODEN bit = 1	
Correct) Pin name	I/O ¹		8.2.1.1 Lis I status* ¹	st of LCD24A Pins	
SEG53-0	A		/ O (L)*2	Segment data output-only pin	
COM7-0	A		./O(L)*2	Common data output-only pin	
SEG71-54	A		0 (L)	General-purpose IO/segment data output pin	
COM23-8	A		0 (L) 0 (L)	General-purpose IO/common data output pin	
LFRO	0		0 (L) 0 (L)	Frame signal monitoring output pin	
Vc1	0		–	LCD panel drive power supply pin	
VC1 VC2	P		_	LCD panel drive power supply pin	
VC2 VC3	<u></u> Р		-	LCD panel drive power supply pin	
VC3 VC4	<u>Р</u>		-		
			-	LCD panel drive power supply pin	
CP1	<u>A</u>		-	LCD voltage booster capacitor connecting pin	
CP2	A		-	LCD voltage booster capacitor connecting pin	
Срз	<u>A</u>		-	LCD voltage booster capacitor connecting pin	
CP4	Α		-	LCD voltage booster capacitor connecting pin	
			pin is confi	gured for LCD24A. *2: When LCD24CTL.MODEN bit = 1	
1C17W34/W35/W30	3 Technical	Manual			
Error)					
				st of LCD32B Pins	
Pin name	I/O*1	Initial status*1		Function	
COM0-15	0			data output-only pins	
SEG0-15/COM16-3	1 0			data output/common data output pins	
SEG16-63	0	Hi-Z / O (L)*2	Segment	data output-only pin	
SEG64-79/COM31-	16 O	Hi-Z / O (L)*2	Segment	data output/common data output pins	
LFRO	0	O (L)		nal monitoring output pin	
	Р	-	LCD pane	I drive power supply pins	
Vc1-Vc5	Α	-	-	ge booster capacitor connecting pins	
	A			igured for LCD32B. *2: When LCD32CTL.LCDDIS bit =	
Cp1-Cp5		atus when the	pin is cont		
Cp1-Cp5		atus when the	pin is conf		
CP1-CP5 *1: Indi			-	st of LCD32B Pins	
CP1-CP5 *1: Indi		Table 1	8.2.1.1 Li	st of LCD32B Pins Function	
CP1-CP5 *1: Indi Correct) Pin name	cates the st	Table 1	8.2.1.1 Li	st of LCD32B Pins	
CP1-CP5 *1: Indi Correct) Pin name COM0-15	cates the st	Table 1 Initial status*1 Hi-Z / O (L)*2	8.2.1.1 Li Common	st of LCD32B Pins Function	
<u>CP1-CP5</u> *1: Indi Correct) <u>Pin name</u> COM0-15 SEG0-15/COM16-3	cates the st	Table 1 Initial status*1 Hi-Z / O (L)*2 Hi-Z / O (L)*2	8.2.1.1 Li Common Segment	st of LCD32B Pins Function data output-only pins data output/common data output pins	
<u>CP1-CP5</u> *1: Indi Correct) <u>Pin name</u> COM0-15 SEG0-15/COM16-3 SEG16-63	II/O ¹	Table 1 Initial status ⁺¹ Hi-Z / O (L) ⁺² Hi-Z / O (L) ⁺² Hi-Z / O (L) ⁺²	8.2.1.1 Li Common Segment Segment	st of LCD32B Pins Function data output-only pins data output/common data output pins data output-only pin	
CP1-CP5 *1: Indi Correct) Pin name COM0-15 SEG0-15/COM16-3 SEG16-63 SEG64-79/COM31-	II/O1 A 1 A A 1 A A 1 A A A 16 A ¹	Table 1 Initial status ¹¹ Hi-Z / O (L) ⁺² Hi-Z / O (L) ⁺² Hi-Z / O (L) ⁺² Hi-Z / O (L) ⁺²	8.2.1.1 Li Common Segment Segment Segment	st of LCD32B Pins Function data output-only pins data output/common data output pins data output-only pin data output/common data output pins	
<u>CP1-CP5</u> *1: Indi Correct) <u>Pin name</u> COM0-15 SEG0-15/COM16-3 SEG16-63 SEG64-79/COM31- LFRO	II/O1 A	Table 1 Initial status ⁺¹ Hi-Z / O (L) ⁺² Hi-Z / O (L) ⁺² Hi-Z / O (L) ⁺²	8.2.1.1 Li Common Segment Segment Segment Frame sig	st of LCD32B Pins Function data output-only pins data output/common data output pins data output-only pin data output/common data output pins nal monitoring output pin	
Correct)	II/O1 A 1 A A 1 A A 1 A A A 16 A ¹	Table 1 Initial status ¹¹ Hi-Z / O (L) ⁺² Hi-Z / O (L) ⁺² Hi-Z / O (L) ⁺² Hi-Z / O (L) ⁺²	8.2.1.1 Li Common Segment Segment Segment Frame sig LCD pane	st of LCD32B Pins Function data output-only pins data output/common data output pins data output-only pin data output/common data output pins	

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ITEM: Treatment of exposed	die pad		
Object manuals	Document codes	Items	Pages
S1C17M01 Technical Manual	412361601	6.7.7 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-16 AP-A-9
S1C17M10 Technical Manual	413180100	6.7.5 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-15 AP-A-9
S1C17M12/M13 Technical Manual	413454200	6.7.6 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-16 AP-A-7
S1C17M30/M31/M32/M33/M34 Technical Manual	413495501	6.7.9 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-31 AP-A-23
S1C17W03/W04 Technical Manual	412924900	6.7.6 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-16 AP-A-10
S1C17W13 Technical Manual	413180301	6.7.6 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-17 AP-A-10
S1C17W14/W16 Technical Manual	412910200	6.7.6 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-17 AP-A-11
S1C17W15 Technical Manual	412645602	6.7.5 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-14 AP-A-9
S1C17W18 Technical Manual	413129501	6.7.10 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-20 AP-A-12
S1C17W22/W23 Technical Manual	412690302	6.7.6 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-16 AP-A-10

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S1C17W34/W35/W36 Technical Manual	413237401	6.7.7 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-17 AP-A-8
S7C17M11 Technical Manual	413393800	6.7.7 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-17 AP-A-8
S1C17589 Technical Manual	412959000	6.7.12 Pd Port Group Appendix A List of Peripheral Circuit Control Registers	6-22 AP-A-7

PDIOEN	15-13	-	0x00	-	R	-
(PD Port Enable	12-8	PDIEN[4:3]	0x0	H0	R/W	
Register)	10	(reserved)	0	H0	R/W	
	9-8	PDIEN[1:0]	0x0	H0	R/W	
	7-5	-	0x00	-	R	
	4-3	PDOEN[4:3]	0x0	H0	R/W	
	2	(reserved)	0	H0	R/W	
	1-0	PDOEN[1:0]	0x0	H0	R/W	
	1 1-0	FDOLN[1.0]	0.00	110		
(Correct)						-
PDIOEN	15-13	-	0x00	_	R	-
PDIOEN (PD Port Enable		- PDIEN[4:3]				-
PDIOEN	<u>15-13</u> <u>12-8</u>	-	0x00 0x0	– H0	R R/W	-
PDIOEN (PD Port Enable	15-13 12-8 10	– PDIEN[4:3] (reserved)	0x00 0x0 0	– H0 H0	R R/W R/W	

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ITEM: SVD Control Object manuals	Document codes	Items	Pages
-			
S1C17W03/W04	412925001	10.4.1 SVD Control	10-3
Technical Manual			
S1C17W13 Technical Manual	413180401	10.4.1 SVD Control	10-3
S1C17W14/W16	412910300	10.4.1 SVD Control	10-3
Technical Manual			
S1C17W15 Technical Manual	412645702	10.4.1 SVD Control	10-3
S1C17W18 Technical Manual	413129601	10.4.1 SVD Control	10-3
S1C17W22/W23	412690402	10.4.1 SVD Control	10-3
Technical Manual			
S1C17W34/W35/W36	413237901	10.4.1 SVD Control	10-3
Technical Manual			
S1C17M01 Technical Manual	412361701	9.4.1 SVD Control	9-3
S1C17M10 Technical Manual	413180200	10.4.1 SVD3 Control	10-3
S7C17M11 Technical Manual	413393900	9.4.1 SVD3 Control	9-3
S1C17589 Technical Manual	412959200	10.4.1 SVD Control	10-3
S1C17M10 Technical Manual, S	S7C17M11 Technica	al Manual	
(Error)			
4. Set the following bits who	en using the inter	rupt:	
- Write 1 to the SVDINTF.	•	•	
- Set the SVDINTE.SDVIE	Υ.	1 0,	
(Correct)			
4. Set the following bits who	en using the inter	rupt:	
- Write 1 to the SVDINTF.	SVDIF bit. (Clear	interrupt flag)	
- Set the SVDINTE. <u>SVDIE</u>	bit to 1. (Enable	SVD3 interrupt)	

(Error)

- 4. Set the following bits when using the interrupt:
- Write 1 to the SVDINTF.SVDIF bit. (Clear interrupt flag)
- Set the SVDINTE.SDVIE bit to 1. (Enable SVD interrupt)

(Correct)

- 4. Set the following bits when using the interrupt:
- Write 1 to the SVDINTF.SVDIF bit. (Clear interrupt flag)
- Set the SVDINTE.<u>SVDIE</u> bit to 1. (Enable SVD interrupt)

	aracteristics	, 					
Object manual		Document code	Object item			F	Page
S7C17W03/W04 Technical	Monuel	412025004	21.9 UART (UART)		2	21-9
S7C17W03/W04 Technical	Manual	412925001	Characteristics				
S1C17W13 Technical Manu	ual	413180401	21.9 UART (UART2)	2	21-10
	lai	413180401	Characteristics				
S1C17W14/16 Technical Manual		412910300	22.9 UART (UART)		2	22-9
S1C17W14/16 Technical Manual		412910300	Characteristi	cs			
S1C17W15 Technical Manual		412645702	20.9 UART (UART)		2	20-9
S1C17W15 Technical Manual		412045702	Characteristi	cs			
		412120604	23.9 UART (UART)		2	23-9
S1C17W18 Technical Manu	iai	413129601	Characteristi	cs			
S1C17W22/W23 Technical Manual		412690402	23.9 UART (UART)		2	23-9
	Mariuai	412090402	Characteristics				
S1C17W13 Technical Manu	Jal						
(Error)							
Unless otherwise specified: VDD =					-	Max.	
Item Transfer baud rate	Symbol UBRT1	Condition Normal mode	VDD 1.6 to 3.6 V	Min. 150	Тур.	230.40	
	Com		1.2 to 1.6 V	150	-	57,60	
	UBRT2	IrDA mode	1.6 to 3.6 V	150	-	57,60	0 bps
			1.2 to 1.6 V	150	-	14,40	0 bps
(Correct)							
Unless otherwise specified: VDD =	1.2 to 3.6 V, Vss	= 0 V , Ta = −40 to 85 ° C					
Item	Symbol	Condition	VDD	Min.	Ţyp.	Max.	Unit
Transfer baud rate	UBRT1	Normal mode	1.6 to 3.6 \	150	-	460,800	
		h D A man da	1.2 to 1.6	150	-	57,600	
	UBRT2	IrDA mode	1.6 to 3.6 \	150 150	-		
			1.2 to 1.6 \	150	-	000	bps
Othera							
Others							

Item	Symbol	Condition	VDD	Min.	Typ.	Max.	Unit
Transfer baud rate	UBRT1	Normal mode	1.6 to 3.6 V	150	-	230,400	bps
			1.2 to 1.6 V	150	-	57,600	bps
	UBRT2	IrDA mode	1.6 to 3.6 V	150	-	57,600	bps
			1.2 to 1.6 V	150	-	14.400	bps
Correct) Jnless otherwise specified: Voo	e = 1.2 to 3.6 V, Vs	s = 0 V, Ta = -40 to 85 °C	II		1		
,	= 1.2 to 3.6 V, Vs Symbol	, -	VDD	Min.	Typ.	Max.	
Jnless otherwise specified: Voo Item	,	, -	Vdd 1.6 to 3.6 V	Min. 150	Typ.		Unit
Jnless otherwise specified: Voo Item	Symbol	Condition				Max.	Unit
Inless otherwise specified: Voo	Symbol	Condition	1.6 to 3.6 V	150		Max. 230,400	Unit bps bps bps

Object manual	Document code	Object item	Page
S1C17M01 Technical Manual	412361701	14.4.3 External Voltage Application Mode 2	14-4
S7C17M11 Technical Manual	413393900	17.4.3 External Voltage Application Mode 2	17-4
S1C17W13 Technical Manual	413180401	18.4.3 External Voltage Application Mode 2	18-4
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S1C17W15 Technical Manual	412645702	17.4.3 External Voltage Application Mode 2	17-4
S1C17W18 Technical Manual	413129601	18.4.3 External Voltage Application Mode 2	18-4
S1C17W22/W23 Technical Manual	412690402	18.4.3 External Voltage Application Mode 2	18-4

(Error)

In this mode, one of the LCD drive voltages VC1 to VC4 are applied from outside the IC and other voltages are internally generated. To put LCD24A into external voltage application mode 2, set the LCD24PWR.VCEN bit to 0 to turn the LCD voltage regulator off and the LCD24PWR.BSTEN bit to 1 to turn the LCD voltage booster on.

(Correct)

In this mode, one of the LCD drive voltages VC1 to <u>VC2</u> are applied from outside the IC and other voltages are internally generated. To put LCD24A into external voltage application mode 2, set the LCD24PWR.VCEN bit to 0 to turn the LCD voltage regulator off and the LCD24PWR.BSTEN bit to 1 to turn the LCD voltage booster on.

S1C17W14/W16, S1C17M01, S7C17M11 Technical Manual

(Error)

In this mode, one of the LCD drive voltages VC1 to VC3 are applied from outside the IC and other voltages are internally generated. To put LCD8B into external voltage application mode 2, set the LCD8PWR.VCEN bit to 0 to turn the LCD voltage regulator off and the LCD8PWR.BSTEN bit to 1 to turn the LCD voltage booster on.

(Correct)

In this mode, one of the LCD drive voltages VC1 to <u>VC2</u> are applied from outside the IC and other voltages

are internally generated. To put LCD8B into external voltage application mode 2, set the LCD8PWR.VCEN bit to 0 to turn the LCD voltage regulator off and the LCD8PWR.BSTEN bit to 1 to turn the LCD voltage booster on.

S1C17W13 Technical Manual

(Error)

In this mode, all the LCD drive voltages VC1 to VC3 are applied from outside the IC. To put LCD4A into external voltage application mode 1, set the LCD4PWR.EXVCSEL bit to 1 and set both the LCD4PWR.VCEN and LCD4PWR.BSTEN bits to 0 to turn both the LCD voltage regulator and LCD voltage booster off.

(Correct)

In this mode, all the LCD drive voltages VC1 to <u>VC2</u> are applied from outside the IC. To put LCD4A into external voltage application mode 1, set the LCD4PWR.EXVCSEL bit to 1 and set both the LCD4PWR.VCEN and LCD4PWR.BSTEN bits to 0 to turn both the LCD voltage regulator and LCD voltage booster off.

ITEM 16bits PWM timer (T16B)			
Object manual	Document code	Object item	Page
S1C17589 Technical Manual	412959200	16bits PWM timer (T16B)	15-5
S1C17M10 Technical Manul	413180200		16-5
S1C17W03/W04Technical manual	412925001		15-5
S1C17W13 Technical Manual	413180401		15-5
S1C17W14/16Technical Manual	412910300		15-5
S1C17W15Technical Manual	412645702		15-5
S1C17W18Technical Manual	413129601		15-5
S1C17W22/W23 Technical Manual	412690402		15-5
S1C17W34/W35/W36 Technical Manual	413237901		15-5
S7C17M11 Technical Manual	413393900		15-5

1.1 Features

(Error)

MAX counter data register

The MAX counter data register (T16B*n*MC.MC[15:0] bits) is used to set the maximum value of the counter (hereafter referred to as MAX value). This setting limits the count range to 0x0000–MAX value and determines the count and interrupt cycles. When the counter is set to repeat mode, the MAX value can be rewritten in the procedure shown below even if the counter is running.

- 1. Check to see if the T16BnCTL.MAXBSY bit is set to 0.
- 2. Write the MAX value to the T16BnMC.MC[15:0] bits.

(Correct)

Add note statement (underlined).

MAX counter data register

The MAX counter data register (T16BnMC.MC[15:0] bits) is used to set the maximum value of the counter (hereafter referred to as MAX value). This setting limits the count range to 0x0000–MAX value and determines the count and interrupt cycles. When the counter is set to repeat mode, the MAX value can be rewritten in the procedure shown below even if the counter is running.

- 1. Check to see if the T16BnCTL.MAXBSY bit is set to 0.
- 2. Write the MAX value to the T16BnMC.MC[15:0] bits.

Note: When rewriting the MAX value, the new MAX value should be written after the counter has been reset to

the previously set MAX value.

ITEM DCLK pin precautions	1		
Object manual	Document code	Object item	Page
S1C17W03/W04 Technical Manual	412925001	3.3.3 List of debugger input/output pins	3-3
S1C17W13 Technical Manual	413180401	3.3.3 List of debugger input/output pins	3-3
S1C17W14/W16 Technical Manual	412910300	3.3.3 List of debugger input/output pins	3-3
S1C17W15 Technical Manual	412645702	3.3.3 List of debugger input/output pins	3-3
S1C17W18 Technical Manual	413129601	3.3.3 List of debugger input/output pins	3-3
S1C17W22/W23 Technical Manual	412690402	3.3.3 List of debugger input/output pins	3-3
S1C17W34/W35/W36 Technical Manual	413237901	3.3.3 List of debugger input/output pins	3-3
S1C17M01 Technical Manual	412361701	3.3.3 List of debugger input/output pins	3-3
S1C17M10 Technical Manual	413180200	3.3.3 List of debugger input/output pins	3-3
S1C17589 Technical Manual	412959200	3.3.3 List of debugger input/output pins	3-3

(Error)

The debugger input/output pins are shared with general-purpose I/O ports and are initially set as the debug pins. If the debugging function is not used, these pins can be switched to general-purpose I/O port pins. For details, refer to the "I/O Ports" chapter.

(Correct)

The debugger input/output pins are shared with general-purpose I/O ports and are initially set as the debug pins. If the debugging function is not used, these pins can be switched to general-purpose I/O port pins. For details, refer to the "I/O Ports" chapter.

Note: The DCLK pin can't drive by high level input from external. (E.g. The pin is done pull-up etc.) Also, the DCLK pin and the other general purpose I/O pins can't connect by a short. Because in both cases, it has possibility that the IC can't work normally by the effect of unstable I/O at power-on.

ITEM I ² C(I2C)			•
Object manual	Document code	Object item	Page
S1C17M01 Technical Manual	412361701	8.6 Control Registers	8-6
S1C17F13 Technical Manual	412486301	8.6 Control Registers	8-6
S1C17W22/W23 Technical Manual	412690402	9.6 Control Registers	9-6
S1C17W15 Technical Manual	412645702	9.6 Control Registers	9-6
S1C17589 Technical Manual	412959200	9.6 Control Registers	9-6
S1C17W14/W16 Technical Manual	412910300	9.6 Control Registers	9-6
S1C17W03/W04 Technical Manual	412925001	9.6 Control Registers	9-6
S1C17W18 Technical Manual	413129601	9.6 Control Registers	9-6
S1C17M10 Technical Manual	413180200	9.6 Control Registers	9-6
S1C17W13 Technical Manual	413180401	9.6 Control Registers	9-6
S1C17W34/W35/W36 Technical	413237901	9.6 Control Registers	9-6
Manual			

(Error)

14.4.3 Data Reception in Master Mode

A data receiving procedure in master mode and the I2C Ch.n operations are shown below. Figures 14.4.3.1 and 14.4.3.2 show an operation example and a flowchart, respectively.

Data receiving procedure

- 1. Issue a START condition by setting the I2CnCTL.TXSTART bit to 1.
- 2. Wait for a transmit buffer empty interrupt (I2CnINTF.TBEIF bit=1) or a START condition interrupt (I2CnINTF.STARTIF bit=1).

Clear the I2CnINTF.STARTIF bit by writing 1 after the interrupt has occurred.

- 3. Write the 7-bit slave address to the I2CnTXD.TXD[7:1] bits and 1 that represents READ as the data transfer direction to the I2CnTXD.TXD0 bit.
- 4. Wait for a receive buffer full interrupt (I2CnINTF.RBFIF bit=1) generated when a one-byte reception has completed or a NACK reception interrupt (I2CnINTF.NACKIF bit=1) generated when a NACK is received.
 - i. Go to Step 5 when a receive buffer full interrupt has occurred.
 - ii. Clear the I2CnINTF.NACKIF bit and issue a STOP condition by setting the I2CnCTL.TXSTOP bit to 1 when a NACK reception interrupt has occurred. Then go to Step 8 or Step 1 if making a retry.
- 5. Perform one of the operations below when the last or next-to-last data is received.
 - i. When the next-to-last data is received, write 1 to the I2CnCTL.TXNACK bit to send a NACK after the last data is received, and then go to Step 6.
 - ii. When the last data is received, read the received data from the I2CnRXD register and set the



14.4.6 Data Reception in Slave Mode

A data receiving procedure in slave mode and the I2C Ch.n operations are shown below. Figures 14.4.6.1 and 14.4.6.2 show an operation example and a flowchart, respectively.

Data receiving procedure

- 1. Wait for a START condition interrupt (I2CnINTF.STARTIF bit=1).
- 2. Check to see if the I2CnINTF.TR bit=0 (reception mode). (Start a data sending procedure if I2CnINTF.TR bit=1.)
- 3. Clear the I2CnINTF.STARTIF bit by writing 1.
- 4. Wait for a receive buffer full interrupt (I2CnINTF.RBFIF bit=1) generated when a one-byte reception has completed or an end of transfer interrupt (I2CnINTF.BYTEENDIF bit=1). Clear the I2CnINTF.BYTEENDIF bit by writing 1 after the interrupt has occurred.
- 5. If the next receive data is the last one, write 1 to the I2CnCTL.TXNACK bit to send a NACK after it is received.



- 2. Issue a START condition by setting the I2CnCTL.TXSTART bit to 1.
- 3. Wait for a transmit buffer empty interrupt (I2CnINTF.TBEIF bit=1) or a START condition interrupt (I2CnINTF.STARTIF bit=1).

Clear the I2CnINTF.STARTIF bit by writing 1 after the interrupt has occurred.

- 4. Write the 7-bit slave address to the I2CnTXD.TXD[7:1] bits and 1 that represents READ as the data transfer direction to the I2CnTXD.TXD0 bit.
- Wait for a receive buffer full interrupt (I2CnINTF.RBFIF bit=1) generated when a one-byte reception has completed or a NACK reception interrupt (I2CnINTF.NACKIF bit=1) generated when a NACK is received.



and 14.4.6.2 show an operation example and a flowchart, respectively.

Data receiving procedure

1.When a one-byte reception, write 1 to the I2CnCTL.TXNACK bit.

- 2. Wait for a START condition interrupt (I2CnINTF.STARTIF bit=1).
- Check to see if the I2CnINTF.TR bit=0 (reception mode).
 (Start a data sending procedure if I2CnINTF.TR bit=1.)
- 4. Clear the I2CnINTF.STARTIF bit by writing 1.
- 5. Wait for a receive buffer full interrupt (I2CnINTF.RBFIF bit=1) generated when a one-byte reception has completed or an end of transfer interrupt (I2CnINTF.BYTEENDIF bit=1).

Clear the I2CnINTF.BYTEENDIF bit by writing 1 after the interrupt has occurred.

- If the next receive data is the last one, write 1 to the I2CnCTL.TXNACK bit to send a NACK after it is received.
- 7. Read the received data from the I2CnRXD register.
- 8. Repeat Steps 5 to 7 until the end of data reception.
- Wait for a STOP condition interrupt (I2CnINTF.STOPIF bit=1) or a START condition interrupt (I2CnINTF.STARTIF bit=1).
 - i. Go to Step 10 when a STOP condition interrupt has occurred.
 - ii. Go to Step 3 when a START condition interrupt has occurred.
- 10. Clear the I2CnINTF.STOPIF bit and then terminate data receiving operations.

Data receiving operations

(abbrev.)



ITEM Real-Time Clock (RTCA)	-	-	_
Object manual	Document code	Object item	Page
S1C17M01 Technical Manual	412361701	8.6 Control Registers	8-6
S1C17F13 Technical Manual	412486301	8.6 Control Registers	8-6
S1C17W22/W23 Technical Manual	412690402	9.6 Control Registers	9-6
S1C17W15 Technical Manual	412645702	9.6 Control Registers	9-6
S1C17589 Technical Manual	412959200	9.6 Control Registers	9-6
S1C17W14/W16 Technical Manual	412910300	9.6 Control Registers	9-6
S1C17W03/W04 Technical Manual	412925001	9.6 Control Registers	9-6
S1C17W18 Technical Manual	413129601	9.6 Control Registers	9-6
S1C17M10 Technical Manual	413180200	9.6 Control Registers	9-6
S1C17W13 Technical Manual	413180401	9.6 Control Registers	9-6
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Manual			

(Error)

Bits14–8 RTCTRM[6:0]

Write the correction value for adjusting the 1 Hz frequency to these bits to execute theoretical regulation.For a calculation method of correction value, refer to "Theoretical Regulation Function." Note: When the RTCCTL.RTCTRMBSY bit = 1, the RTCCTL.RTCTRM[6:0] bits cannot be rewritten.

(Correct)

Bits14–8 RTCTRM[6:0]

Write the correction value for adjusting the 1 Hz frequency to these bits to execute theoretical regulation.For a calculation method of correction value, refer to "Theoretical Regulation Function."

Notes: When the RTCCTL.RTCTRMBSY bit = 1, the RTCCTL.RTCTRM[6:0] bits cannot be rewritten.
When 0x00 is written to the RTCCTL.RTCTRM[6:0] bits, the RTCCTL.RTCTRMBSY bit goes 1, but the time-of-day clock is not corrected.

Object manual		Document code	Object item	Page
S1C17M01 Technical	Manual	412361701	7.4 Control Registers	7-3~4
S1C17F13 Technical	Manual	412486301	7.4 Control Registers	7-3~4
S1C17W22/W23 Tech	nnical Manual	412690402	8.4 Control Registers	8-3~4
S1C17W15 Technical	Manual	412645702	8.4 Control Registers	8-3~4
S1C17589 Technical	Manual	412959200	8.4 Control Registers	8-3~4
S1C17W14/W16 Tech	nnical Manual	412910300	8.4 Control Registers	8-3~4
S1C17W03/W04 Tech	nnical Manual	412925001	8.4 Control Registers	8-3~4
S1C17W18 Technical	Manual	413129601	8.4 Control Registers	8-3~4
0xa (R/WP): Values other than 0 Always 0x0 is read				
Values other than 0 Always 0x0 is read	if a value other be generated in	than 0xa is written. nmediately after run	ning depending on the counter	⁻ value, WDT
Values other than C Always 0x0 is read Since a reset may b should also be rese (Correct)	if a value other be generated in et concurrently v	than 0xa is written. nmediately after run	ning depending on the counter	⁻ value, WDT
Values other than C Always 0x0 is read Since a reset may b should also be rese (Correct) Bits 3–0 WDTRUN[if a value other be generated in et concurrently v	than 0xa is written. nmediately after run when running WDT.	ning depending on the counter	⁻ value, WDT
Values other than 0 Always 0x0 is read Since a reset may b should also be rese (Correct) Bits 3–0 WDTRUN[These bits control V	if a value other be generated in et concurrently v (3:0] WDT to run and	than 0xa is written. nmediately after run when running WDT.	ning depending on the counter	⁻ value, WDT
Values other than 0 Always 0x0 is read Since a reset may b should also be rese (Correct) Bits 3–0 WDTRUN[These bits control V 0xa (WP):	if a value other be generated in et concurrently v (3:0] WDT to run and Stop	than 0xa is written. nmediately after run when running WDT.	ning depending on the counter	⁻ value, WDT
Values other than 0 Always 0x0 is read Since a reset may b should also be rese (Correct) Bits 3–0 WDTRUN[These bits control V	if a value other be generated in et concurrently v (3:0] WDT to run and Stop	than 0xa is written. nmediately after run when running WDT.	ning depending on the counter	[·] value, WDT

ITEM External connection for	VPP		
Object manual	Document code	Object item	Page
S1C17M01 Technical Manual	412361701	4.3.3 Flash Programming	4-3
		17.2 Recommended Operating Conditions	17-1
		18 Basic External Connection Diagram	18-1
S1C17W03/04 Technical Manual	412925001	4.3.3 Flash Programming	4-3
		21.2 Recommended Operating Conditions	21-1
		22 Basic External Connection Diagram	22-1
S1C17W14/16 Technical Manual	412910300	4.3.3 Flash Programming	4-3
		22.2 Recommended Operating Conditions	22-1
		23 Basic External Connection Diagram	23-1
S1C17W15 Technical Manual	412645702	4.3.3 Flash Programming	4-3
		20.2 Recommended Operating Conditions	20-1
		21 Basic External Connection Diagram	21-1
S1C17W22/23 Technical Manual	412690402	4.3.3 Flash Programming	4-3
		23.2 Recommended Operating Conditions	23-1
		24 Basic External Connection Diagram	24-1
S1C17589 Technical Manual	412959200	4.3.3 Flash Programming	4-3
		19.2 Recommended Operating Conditions	19-1
		20 Basic External Connection Diagram	20-1
S1C17656 Technical Manual	412745100	3.2.2 Flash Programming	3-2
Flash Programming			
(Error) (S1C17M01)	(Ex	clude S1C17M01,S1C17656)	
SICI7 SICI7 SRDBG (S	Dmini 5U1C17001H) S1	DCLK	
	2		
VPP C Flast	Vcc OUT		
Figure 4.3.3.1 External Conn	ection F	igure 4.3.3.1 External Connection	
The VPP pin must be left open exce	pt when programm	ing the Flash memory. However, it is not ne	ecessary t
disconnect the wire when using ICD	mini to supply the V	/PP power, as ICDmini controls the power	supply so

that it will be supplied during Flash programming only. CVPP should be connected if the VPP voltage is not



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ITEM The operation when "Display Off" is selected			
Object manual	Document code	Object item	Page
S1C17M01 Technical Manual	412361701	17.5.2 Display On/Off	17-6
S1C17W22/W23 Technical Manual	412690402	18.5.2 Display On/Off	18-7
S1C17W15 Technical Manual	412645702	17.5.2 Display On/Off	17-6
S1C17W14/W16 Technical Manual	412910300	18.5.2 Display On/Off	18-6

(Error)

When "Display off" is selected, the drive voltage supply stops and the LCD driver pin outputs are all set to VSS level.

Since "All on" and "All off" directly control the driving waveform output by the LCD driver, data in the display data RAM is not altered. The common pins are set to dynamic drive for "All on" and to static drive for "All off." This function can be used to make the display flash on and off without altering the display memory.

(Correct)

When "Display off" is selected, the drive voltage supply stops and the LCD driver pin outputs are all set to VSS level.

Since "All on" and "All off" directly control the driving waveform output by the LCD driver, data in the display data RAM is not altered. The common pins are set to dynamic drive for "All on" and to static drive for "All off." This function can be used to make the display flash on and off without altering the display memory.

Note:

When "Display off" is selected, VC4 (or VC3)'s electric charge must be discharged with the procedure shown below.

<Using Internal Generation Mode>

- 1. Set the LCD8PWR.VCEN bit to 0. (Disable LCD voltage regulator)
- 2. Set the LCD8PWR.HVLD bit to 1. (Enable heavy load protection mode)
- When CLK LCDxx is stopped, it must be stopped after VC4 (or VC3)'s electric potential became less than VDD – 1V.

<Using External Voltage Application Mode>

- 1. Disable the external voltage.
- 2. Set the LCD8PWR.HVLD bit to 1. (Enable heavy load protection mode)
- 3. When CLK_LCDxx is stopped, it must be stopped after VC4 (or VC3)'s electric potential became less

<u>than VDD – 1V.</u>

When "Display on" is selected again, it should be in a reverse procedure of the above description.