STW20N95DK5, STWA20N95DK5

N-channel 950 V, 0.275 Ω typ., 18 A, MDmesh™ DK5 Power MOSFETs in TO-247 and TO-247 long leads packages

Datasheet - production data

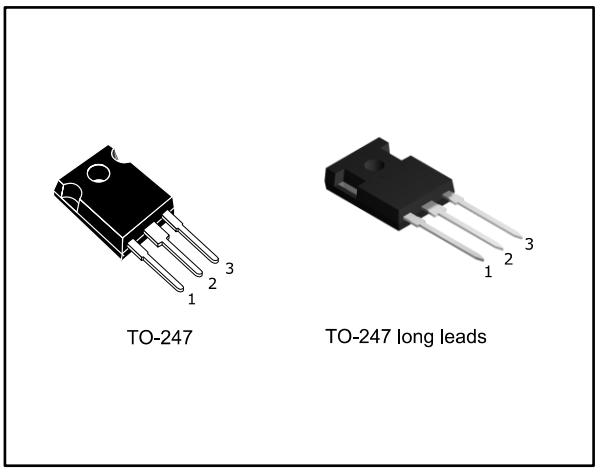
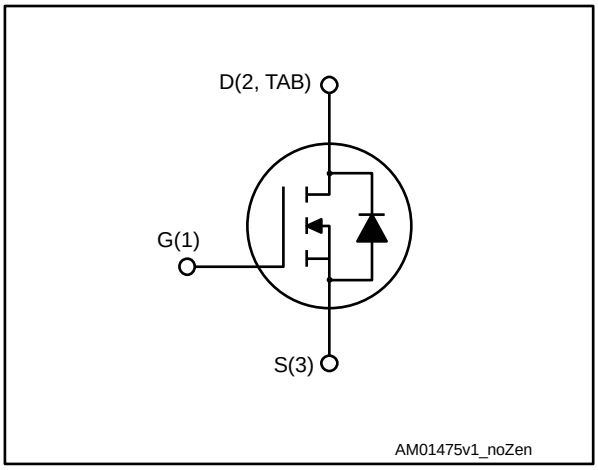


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STW20N95DK5	950 V	0.330 Ω	18 A
STWA20N95DK5			

- Fast-recovery body diode
- Best $R_{DS(on)}$ x area
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are part of the MDmesh™ DK5 fast recovery diode series. The MDmesh™ DK5 combines very low recovery charge (Q_{rr}) and recovery time (t_{rr}) with an excellent improvement in $R_{DS(on)}$ * area and one of the most effective switching behaviors, ideal for half bridge and full bridge converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STW20N95DK5	20N95DK5	TO-247	Tube
STWA20N95DK5		TO-247 long leads	

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	18	V
I_D	Drain current (continuous) at T_C = 100 °C	11	A
I_{DM}(1)	Drain current (pulsed)	72	A
P_{TOT}	Total dissipation at T_C = 25 °C	250	W
dv/dt(2)	Peak diode recovery voltage slope	50	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

Notes:

(1)Pulse width limited by safe operating area

(2)I_{SD} ≤ 8.5 A, di/dt ≤ 400 A/µs, V_{DS} peak ≤ $V_{(BR)DSS}$, V_{DD} = 475 V

(3)V_{DS} ≤ 760 V

Table 3: Avalanche characteristics

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	50	°C/W

Table 4: Thermal data

Symbol	Parameter	Value	Unit
I_{AR}	Maximum current during repetitive or single pulse avalanche	6	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR} ,V_{DD} = 50 V)	520	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0 V	950			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 950 V			10	µA
		V_{GS} = 0 V, V_{DS} = 950 V, T_C= 125 °C (1)			100	µA
I_{GSS}	Gate source leakage current	V_{DS} = 0 V, V_{GS} = ± 20 V			±2	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DD} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 9 A		0.275	0.330	Ω

Notes:

(1)Defined by design, not subject to production test

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS}= 0 V	-	1600	-	pF
C_{oss}	Output capacitance		-	76	-	pF
C_{rss}	Reverse transfer capacitance		-	5	-	pF
$C_{o(tr)}$(1)	Time- related equivalent capacitance	V_{GS} = 0 V, V_{DS}= 0 to 760 V	-	169	-	pF
$C_{o(er)}$(2)	Energy-related equivalent capacitance		-	60	-	pF
R_g	Intrinsic gate resistance	f =1 MHz, I_D= 0 A	-	4	-	Ω
Q_g	Total gate charge	V_{DD} = 760 V, I_D = 18 A, V_{GS} = 0 to 10 V (see *Figure 16: "Test circuit for gate charge behavior"*)	-	50.7	-	nC
Q_{gs}	Gate source charge		-	7.8	-	nC
Q_{gd}	Gate drain charge		-	34.2	-	nC

Notes:

(1)$C_{o(tr)}$ is defined as the constant equivalent capacitance giving the same charging time as Coss when V_{DS} increases from 0 to 80% V_{DSS}.

(2)$C_{o(er)}$ is defined as the constant equivalent capacitance giving the same stored energy as Coss when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DS} = 475 V, I_D= 9 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 15: "Test circuit for resistive load switching times"* and *Figure 20: "Switching time waveform"*)	-	23	-	ns
t_r	Rise time		-	23	-	ns
$t_{d(off)}$	Turn-off delay time		-	74	-	ns
t_f	Fall time		-	25.4	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		18	A
I_{SDM}(1)	Source-drain current (pulsed)		-		72	A
V_{SD}(2)	Forward on voltage	I_{SD} = 18 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 9 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"*)	-	150		ns
Q_{rr}	Reverse recovery charge		-	1		µC
I_{RRM}	Reverse recovery current		-	13.5		A
t_{rr}	Reverse recovery time	I_{SD} = 9 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 17: "Test circuit for inductive load switching and diode recovery times"*)	-	264		ns
Q_{rr}	Reverse recovery charge		-	2.9		µC
I_{RRM}	Reverse recovery current		-	22		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

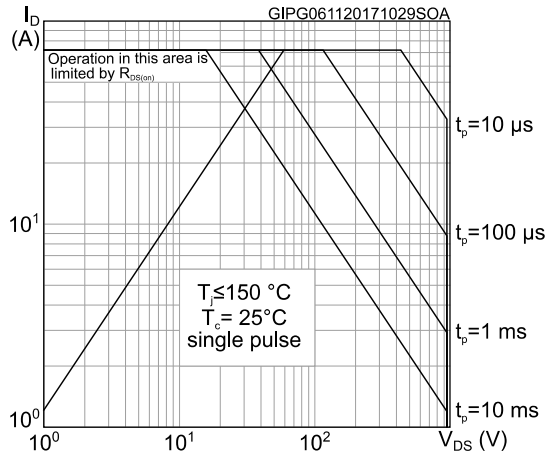


Figure 3: Thermal impedance

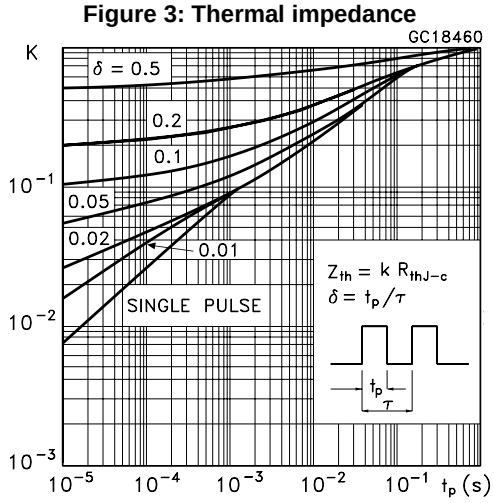


Figure 4: Output characteristics

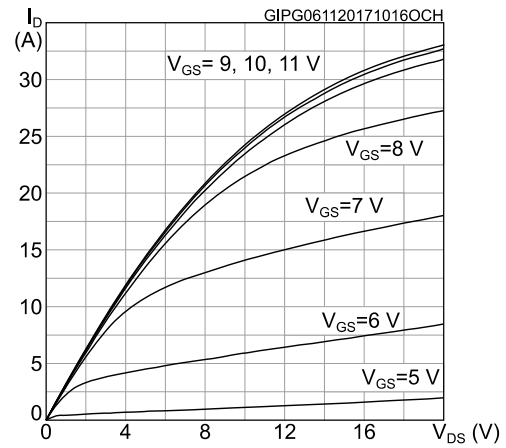


Figure 5: Transfer characteristics

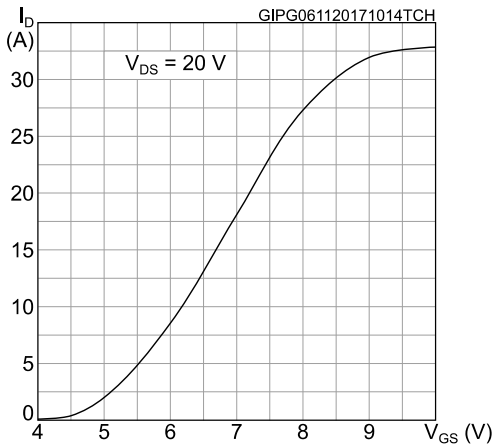


Figure 6: Gate charge vs gate-source voltage

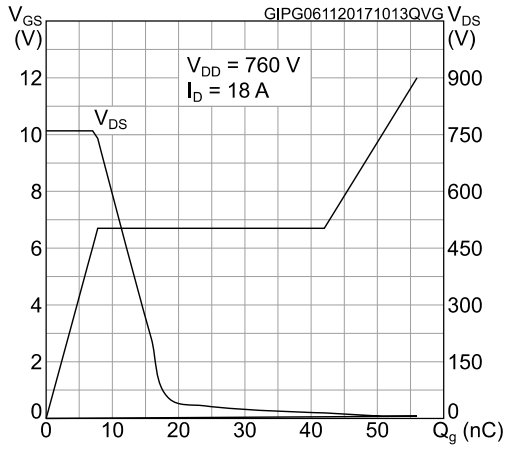


Figure 7: Static drain-source on-resistance

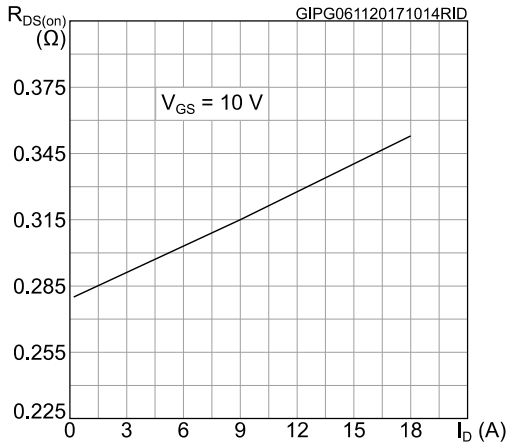


Figure 8: Capacitance variations

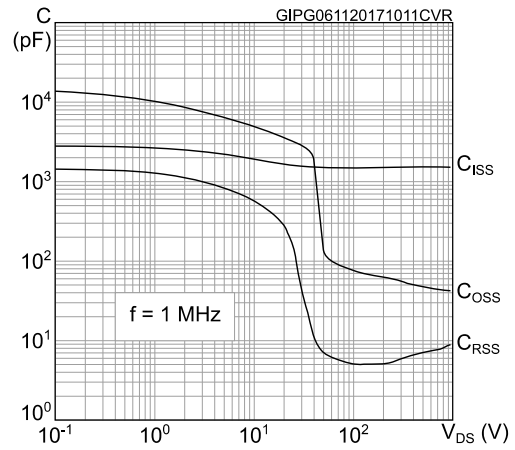


Figure 9: Output capacitance stored energy

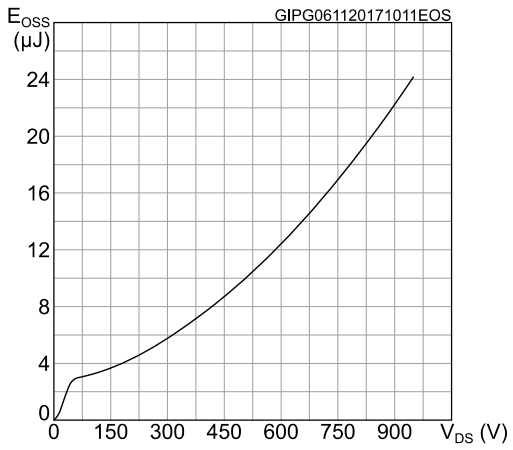


Figure 10: Normalized gate threshold voltage vs temperature

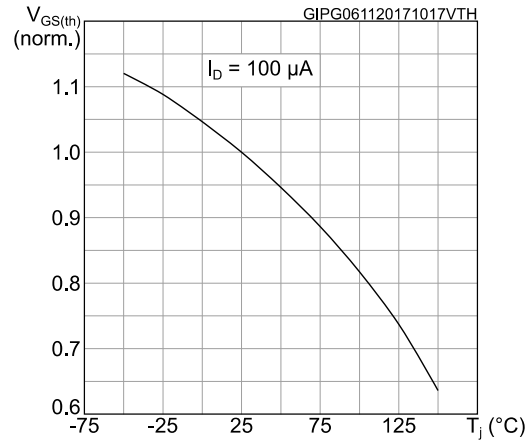


Figure 11: Normalized on-resistance vs temperature

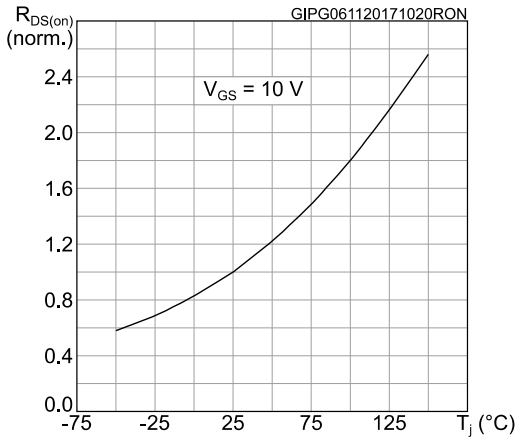


Figure 12: Normalized $V_{(BR)DSS}$ vs temperature

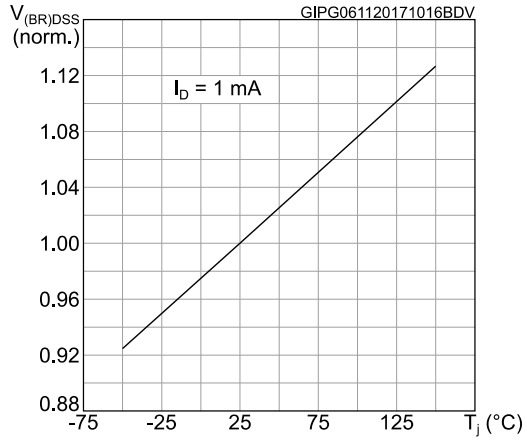


Figure 13: Source-drain diode forward characteristics

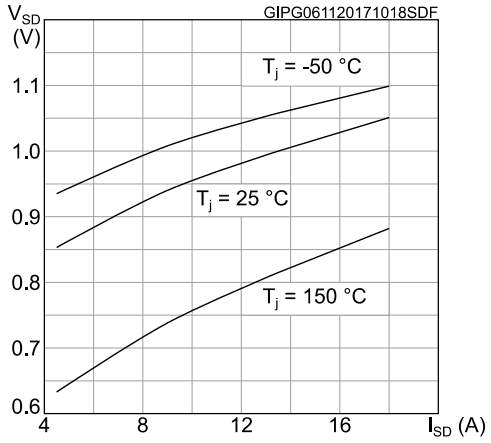
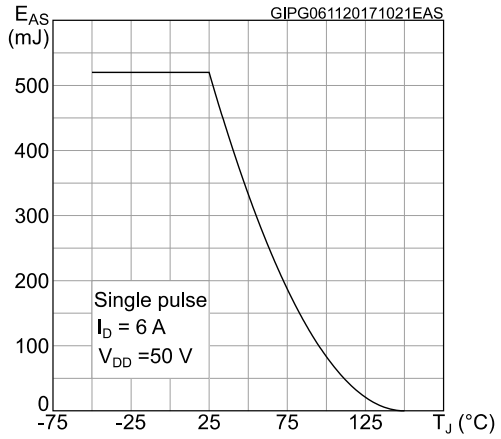


Figure 14: Maximum avalanche energy vs starting T_J



3 Test circuits

Figure 15: Test circuit for resistive load switching times

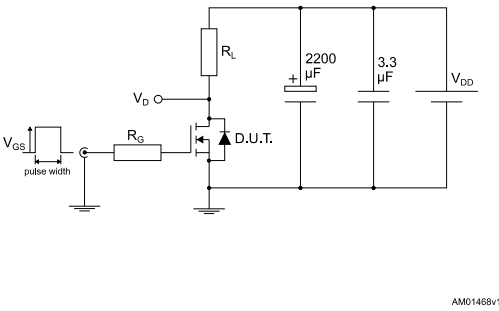


Figure 16: Test circuit for gate charge behavior

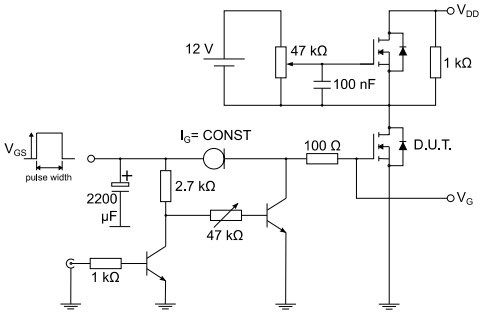


Figure 17: Test circuit for inductive load switching and diode recovery times

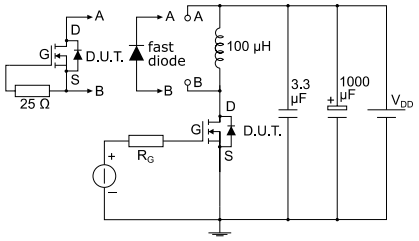


Figure 18: Unclamped inductive load test circuit

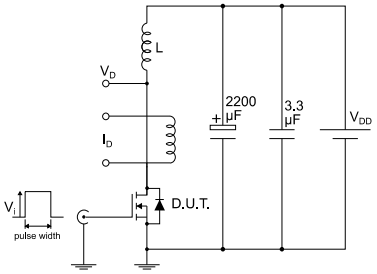


Figure 19: Unclamped inductive waveform

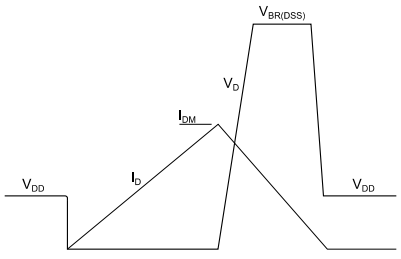
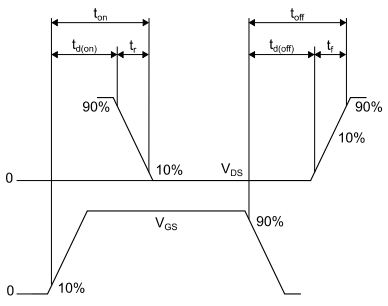


Figure 20: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-247 package information

Figure 21: TO-247 package outline

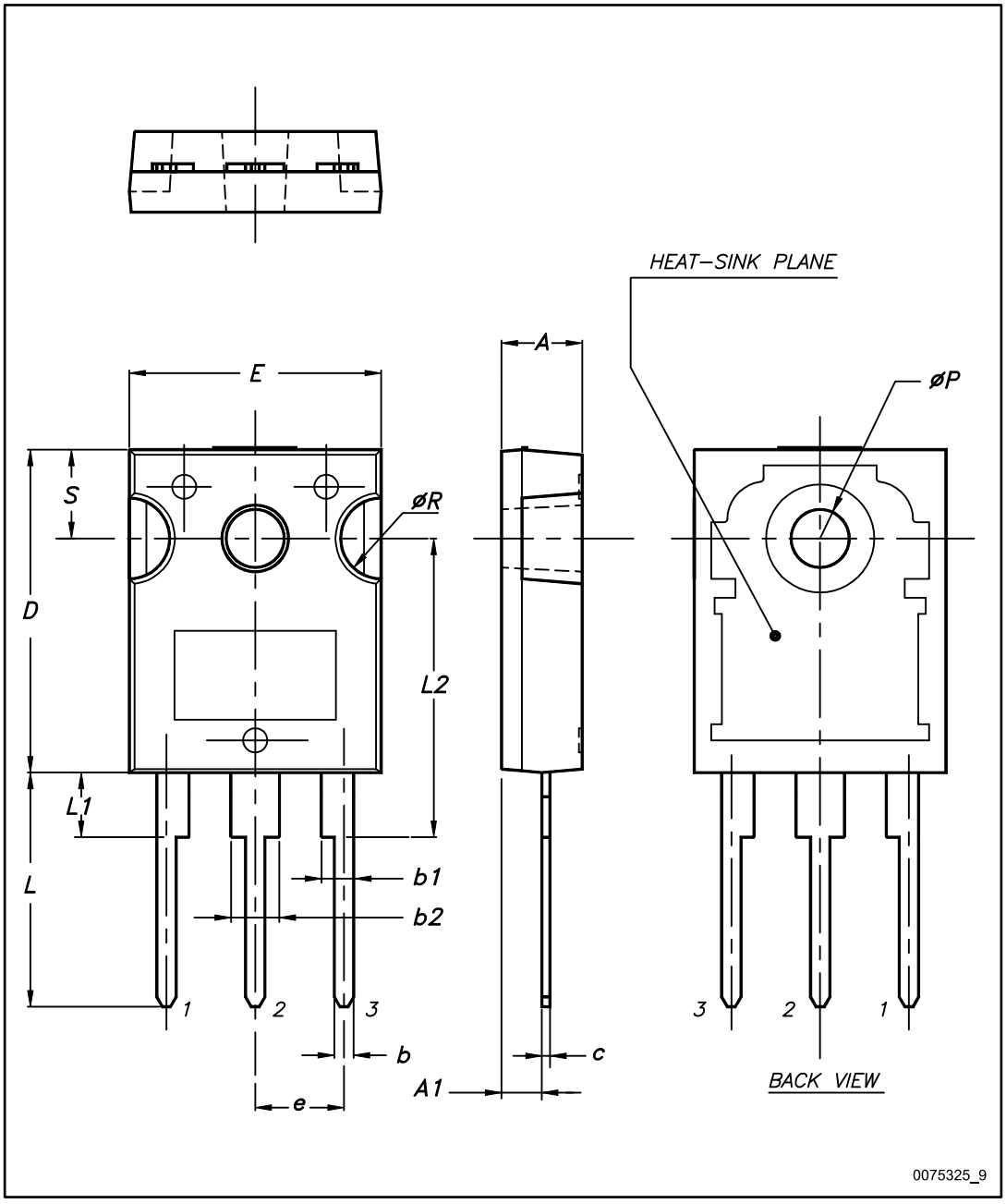


Table 9: TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

4.2 TO-247 long leads package information

Figure 22: TO-247 long leads package outline

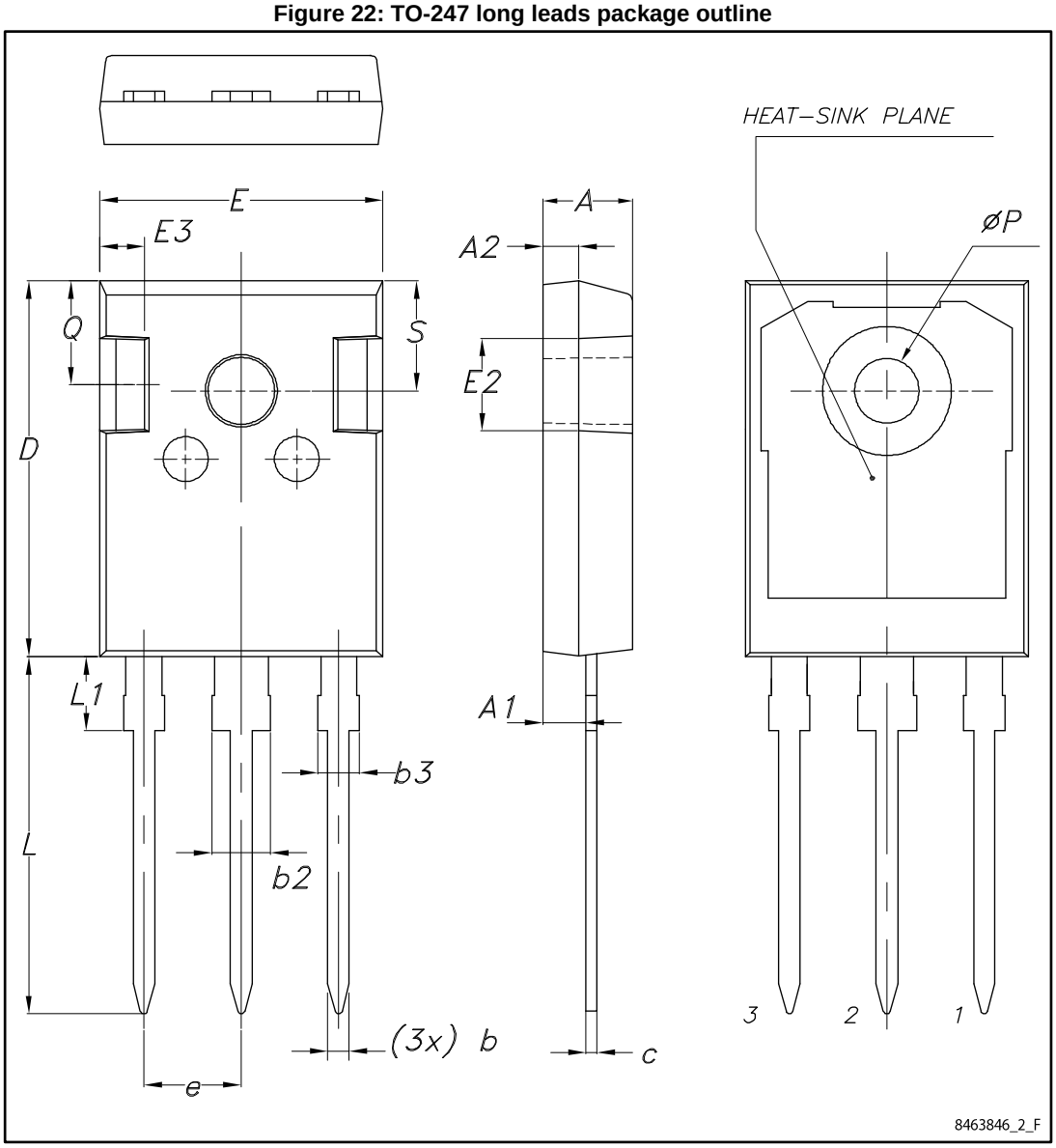


Table 10: TO-247 long leads package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
c	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
P	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
10-May-2017	1	Initial release
06-Nov-2017	2	Datasheet promoted from preliminary data to production data. Modified title and features table on cover page Modified *Table 2: "Absolute maximum ratings"*, *Table 4: "Thermal data"*, *Table 5: "On/off states"*, *Table 6: "Dynamic"*, *Table 7: "Switching times"* and *Table 8: "Source-drain diode"*. Added *Section 2.1: "Electrical characteristics (curves)".* Minor text changes.

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